Module-4

Power Amplifier

The amplifiers in multistage amplifier near the load end in almost all-electronic system employ large signal amplifiers (Power amplifiers) and the purpose of these amplifiers is to obtain power again.

Consider the case of radio receiver, the purpose of a radio receiver is to produce the transmitted programmes with sufficient loudness. Since the radio signal received at the receiver output is of very low power, therefore, power amplifiers are used to put sufficient power into the signal. But these amplifier need large voltage input.

Therefore, it is necessary to amplify the magnitude of input signal by means of small amplifiers to a level that is sufficient to drive the power amplifier stages.

In multistage amplifier, the emphasis is on power gain in amplifier near the load. In these amplifies, the collector currents are much larger because the load resistances are small (i.e impedence of loud speaker is 3.2 ohm).

A power amplifier draws a large amount of dc power form dc source and convert it into signal power. Thus, a power amplifier does not truly amplify the signal power but converts the dc power into signal power.

DC and AC load lines:

Consider a CE amplifier as shown in **fig. 1**.

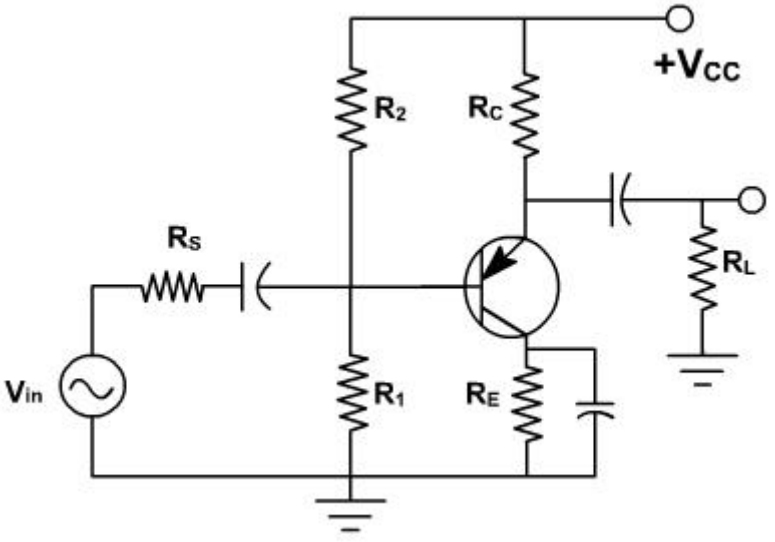

Fig. 1

The dc equivalent circuit gives the dc load line as shown in **fig. 2**.

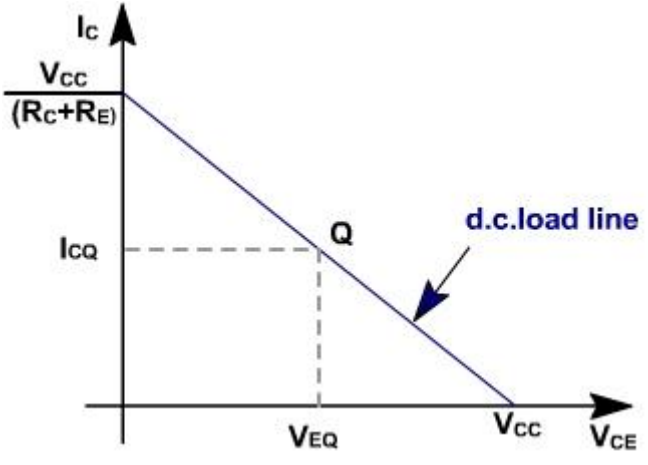

Fig. 2

Q is the operative point. I_{CQ} and V_{CEQ} are quiescent current and voltage. The ac equivalent circuit is shown in **fig. 3**.

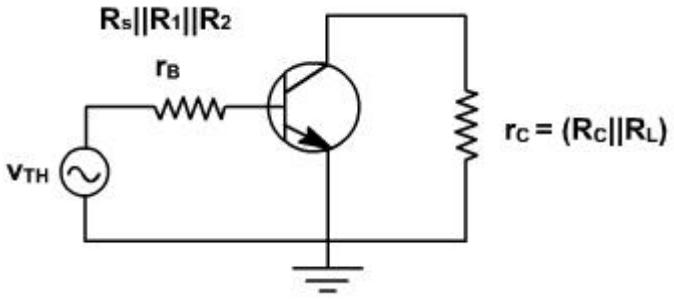

Fig. 3

This circuit produces ac load line. When no signal is present, the transistor operates at the Q point shown in **fig. 4**.

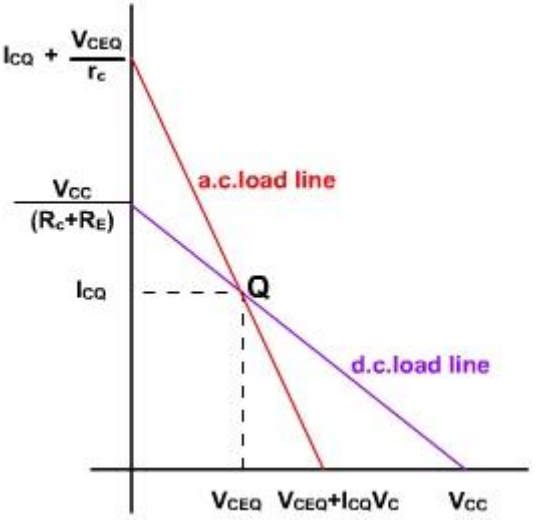

Fig. 4

When a signal is present, operating point swings along the ac load line rather than dc load line. The saturation and cut off points on the ac load line are different from those on the dc load line.

$$V_{ce} + i_c r_c = 0$$

or

$$i_c = -\frac{V_{ce}}{r_c}$$

The ac collector current is given by

$$i_c = I_C - I_{CQ}$$

$$V_{ce} = V_{CE} = V_{CE} - V_{CEQ}$$

$$I_C = I_{CQ} + \frac{V_{CEQ}}{r_c} + \frac{V_{CE}}{r_c}$$

when, $V_{CE} = 0$, $I_C = I_{CQ} + \frac{V_{CEQ}}{r_c}$

when, $I_C = 0$, $V_{CE} = V_{CEQ} + r_c I_{CQ}$

During the positive half cycle of ac source, voltage, the collector voltage swing from the Q-point towards saturation. On the negative cycle, the collector voltage swings from Q-point towards cutoff. For a large signal clipping can occur on either side or both sides.

The maximum positive swing from the Q-point is

$V_{CEQ} + I_{CQ} r_C$ ⇒ $V_{CEQ} = I_{CQ} r_C$.

The maximum negative swing from the Q-point is

0 ⇒ $V_{CEQ} = - V_{CEQ}$.

The ac output compliance (maximum peak to peak unclipped voltage) is given by the smaller of these two approximate values:

$PP = 2 I_{CQ} r_C$

or $PP = 2 V_{CEQ}$.

Class A operation:

In a class ‘A' operation transistor operates in active region at all times. This implies that collector current flows for 360° of the ac cycle.

Voltage gain of loaded amplifier

$$A_V = \frac{r_c}{r'_e}$$

Current gain

$$A_i = \frac{i_c}{i_b} = \beta$$

ac input power to the base $P_{in} = V_{in}\, i_b$

ac output power point = $- V_{out} * i_C$. (Negative sign is due to phase inversion.)

$$A_p = \frac{P_{out}}{P_{in}} = \frac{V_{out}}{V_{in}} * \frac{i_C}{i_b}$$

$$A_p = -A_v A_i$$

The ac power into a load resistor R_L is

$$P_L = \frac{V_L^2}{R_L}$$

Where V_L = rms load voltage

$$\therefore V_L = 0.707\, V_p$$

$$V_p = \frac{V_{PP}}{2}$$

$$\therefore P_L = \left(\frac{0.707 * V_{PP}}{2}\right) * \frac{1}{R_L}$$

$$= \frac{V_{PP}^2}{8R_L}$$

The variation of P_L with V_{PP} is shown in **fig. 5**. Maximum ac load power is obtained when the output unclipped voltage equals ac output compliance PP.

$$\therefore P_{L(max)} = \frac{PP^2}{8R_L}$$

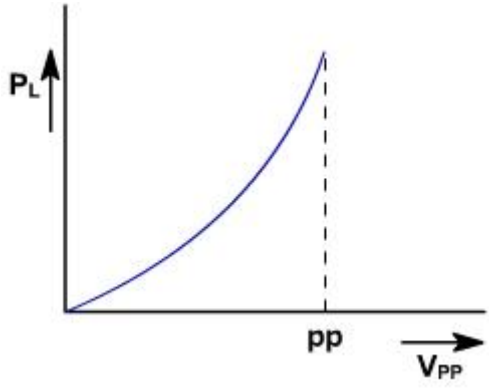

Fig. 5

When no signal drives the amplifier, the power dissipation of the transistor equals the product of d. voltage and current

$P_{DQ} = V_{CEQ} * I_{CQ}$

When there is no input signal, P_D is maximum as shown in **fig. 6**.

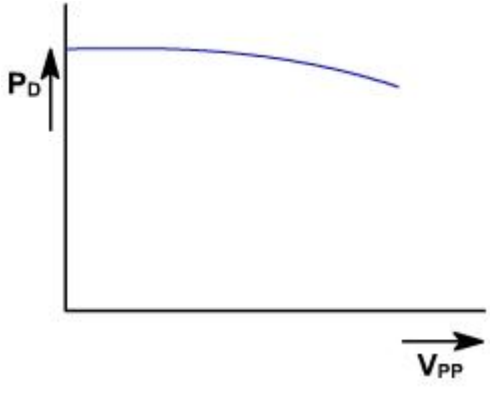

Fig. 6

It decreases when the peak to peak load voltage increases. The power dissipation must be less than the rating of transistor, otherwise temperature increases and transistor may damage. To reduce the temperature, heat sinks are used that dissipates the heat produced. When Q-point is at the center of ac load line then peak swing above and below Q-point is equal.

$$V_P = V_{CEQ} = i_{CQ} * r_C$$

$$\therefore P_D = \frac{V_P^2}{2 * r_C}$$

$$= \frac{V_{CEQ} * I_{CQ} * r_C}{2 * r_C}$$

$$= \frac{V_{CEQ} * I_{CQ}}{2}$$

$$= \frac{P_{DQ}}{2}$$

Class A current drain:

In a class A amplifier shown in **fig.1**, the dc source V_{CC} must supply direct current to the voltage divider and the collector circuit.

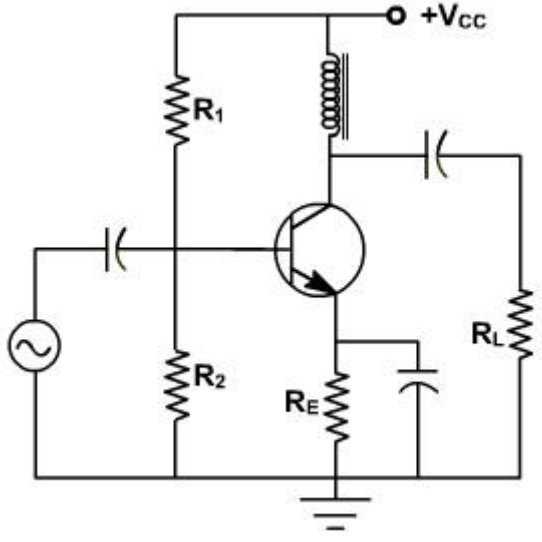

Fig. 1

Assuming a stiff voltage divider circuit, the dc current drain of the voltage divider circuit is

$I_1 = V_{CC} / (R_1 + R_2)$

In the collector circuit, the dc current drain is

$I_2 = I_{CQ}$

In a class A amplifier, the sinusoidal variations in collector current averages to zero. Therefore, whether the ac signal is present or not, the dc source must supply an average current of

$I_S = I_1 + I_2$.

This is the total dc current drain. The dc source voltage multiplied by the dc current drain gives the ac power supplied to an amplifier.

$P_S = V_{CC} I_S$

Therefore, efficiency of the amplifier, $\eta = (P_{L(max)} / P_S) * 100\ \%$

Where,, $P_{L(max)}$ = maximum ac load line power. In class A amplifier, there is a wastage of power in resistor R_C and R_E i.e. $I_{CQ}^2 * (R_C + R_E)$.

To reduce this wastage of power R_C and R_E should be made zero. R_E cannot be made zero because this will give rise to bias stability problem. R_C can also not be made zero because effective load resistance gets shorted. This results in more current and no power transfer to the load R_L. The R_C resistance can, however, be replaced by an inductance whose dc resistance is zero and there is no dc voltage drop across the choke as shown in **fig. 1**.

Since in most application the load is loudspeaker, therefore power amplifier drives the loudspeaker, and the maximum power transfer takes place only when load impedence is equal to the source impedence. If it is not, the loud speaker gets less power. The impedence matching is done with the help of transformer, as shown in **fig. 2**.

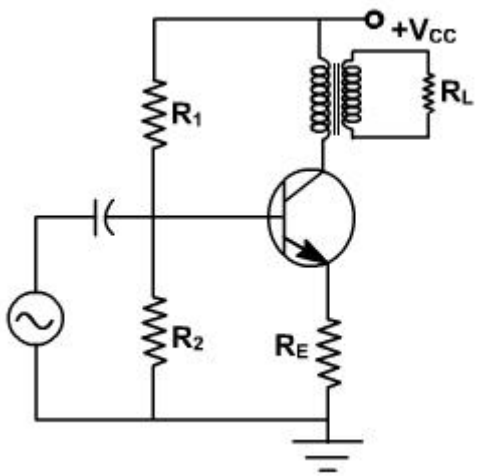

Fig. 2

The ratio of number of turns is so selected that the impedence referred to primary side can be matched with the output impedence of the amplifier.

$$\frac{R_L'}{R_L} = \frac{V_1/I_1}{V_2/I_2} = \left(\frac{V_1}{V_2}\right)\left(\frac{I_2}{I_1}\right) = \left(\frac{N_1}{N_2}\right)^2$$

$$\therefore R_L' = R_L\left(\frac{N_1}{N_2}\right)^2$$

Class B amplifier:

The efficiency (□) of class A amplifier is poor. The reason is that these circuits draw considerable current from the supply even in the absence of input signals.

In class B operation the transistor collector current flows for only 180° of the ac cycle. This implies that the Q-point is located approximately at cutoff on both dc and ac load lines. The advantages of class B operation are

- Lower transistor power dissipation
- Reduced current drain.
- Eficiency is given by

$$\eta_{(max)} = \frac{P_{ac}}{P_{dc}} = \frac{2V_{CC}\,2I_C}{8V_{CC}I_C} \times 100\%$$

- Value is around 70%

Push pull circuit:

When a transistor operates in class B, it clips off a half cycle. To avoid the resulting distortion, two transistors are used in push pull arrangement. This means that one transistor conducts during positive half cycle and other

Fig. 3

transistor conducts during negative half cycle. The distortion is low, load power is large and efficiency (□ □) is more. **fig. 3**, shows how a npn and pnp transistor emitter followers are connected in push pull arrangement.

The dc & ac equivalent circuit are shown in **fig. 4** & **fig. 5**. The biasing resistors are selected so that Q-point is set at cutoff. This biases the emitter diode of each transistor between 0.6V and 0.7V

i.e. $I_{CQ} = 0$.

Because the biasing resistors are equal each emitter diode is biased with the same voltage. As a result half the supply voltage is dropped across each transistor.

$V_{CEQ} = V_{CC} / 2$.

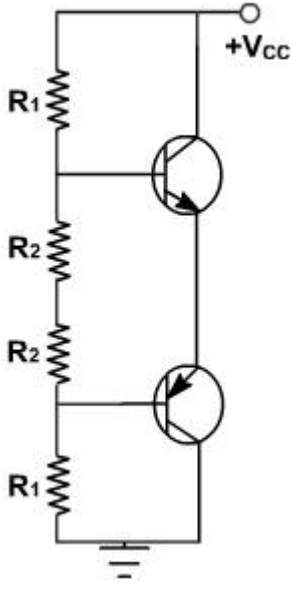

Fig. 4

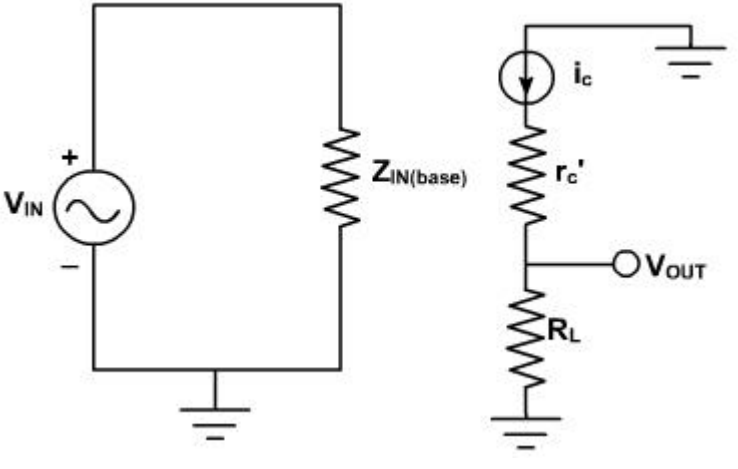

Fig. 5

Since there is no dc resistance in the collector or emitter circuits, the dc saturation current is infinite. The dc load line is vertical as shown in **fig. 6**. The most difficult thing is setting up a stable Q-point at cut off. Any significant increase in V_{BE} with temperature can move the Q-point up the dc load line to dangerously high currents. Ac load line is given by

$I_{C(sat)} = I_{CQ} + (V_{CEQ} / r_E)$

$V_{CE\ (cut\ off)} = V_{CEQ} + I_{CQ}\, r_E$

$I_{CQ} = 0$; $V_{CEQ} = V_{CC} / 2$

i.e. $I_{C(sat)} = V_{CC} / 2R_L$ (i.e. $r_E = R_L$)

$V_{CE\ (cut\ off)} = V_{CC} / 2.$

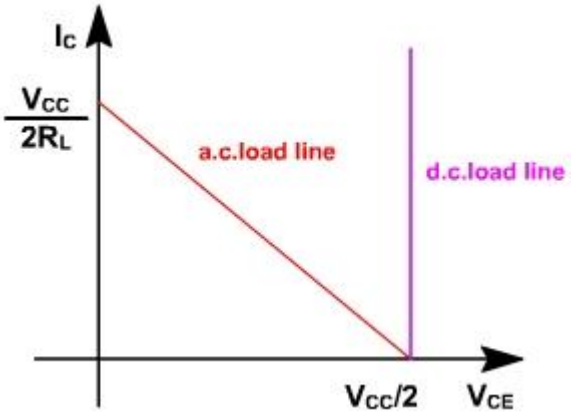

Fig. 6

When either transistor is conducting, that transistor's operating point swings along the ac load line and the operating point of the other transistor remains at cut off. The voltage swing of the conducting transistor can go from cut off to saturation. In the next half cycle, the other transistor does the same thing.

Therefore, $PP = V_{CC}$

Voltage gain of loaded amplifier:

$A_V = R_L / (R_L + r'_e)$

$Z_{in\ (base)}$ □ □ □$(R_L + r'_e)$

$Z_{out} = r'_e + (r_B) /$□ □

$A_P = A_V * A_i$

Without signal the capacitor charges up to $V_{CC} / 2$ relative to ground.

In the positive half cycle of input voltage, the upper transistor conducts and the lower one cut off. The upper transistor acts like an ordinary emitter follower, so that the output voltage

approximately equals the input voltage. The current flow through R_L is such as direct as to make output positive.

In the negative half cycle of input voltage, the upper transistor cuts off and the lower transistor conducts. The lower transistor acts like an ordinary emitter follower and produces a load voltage approximately equal to the input voltage (i.e. negative output. Since Q, is off, no current can flow from V_{CC} through Q, but capacitor acts like a battery source and discharges).

During either half cycle, the source sees a high input impedence looking into either base and the load sees a low output impedence.

Cross over distortion:

Fig. 1 shows the ac equivalent circuit of a class B push pull amplifier. Suppose that no bias is applied to the emitter diodes. Then the incoming voltage has to rise to about 0.7 V to overcome the barrier potential. Because of this no current flows through Q, when the signal is less than 0.7 V. The action is similar on the other half cycle no current flows in Q_2 until ac voltage is more negative the **-** 0.7 V. If no bias is applied the output of class B amplifier looks like as shown in **fig. 1.**

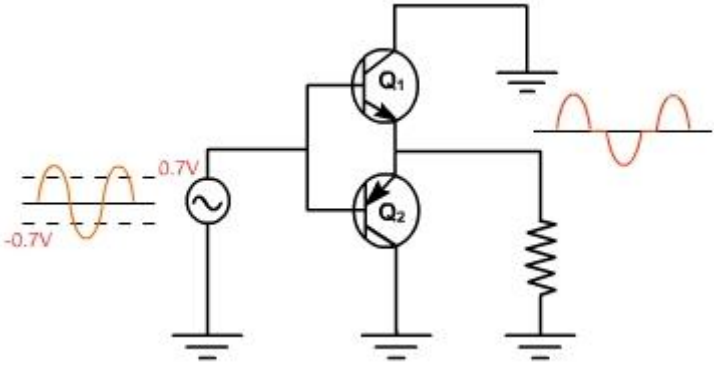

Fig. 1

The signal output is distorted. Because of clipping action between half cycles, it no longer is a sine wave. Since the clipping occurs between the time one transistor cuts off and the time the other comes on, it is called cross over distortion. To eliminate cross over distortion, the slight forward bias must be applied to each emitter diode. This means locating the Q-point

slightly above cut off as shown in **fig. 2**. In fact, this is class AB operation. This means that collector current flows for more than 180 degrees but less than 360°.

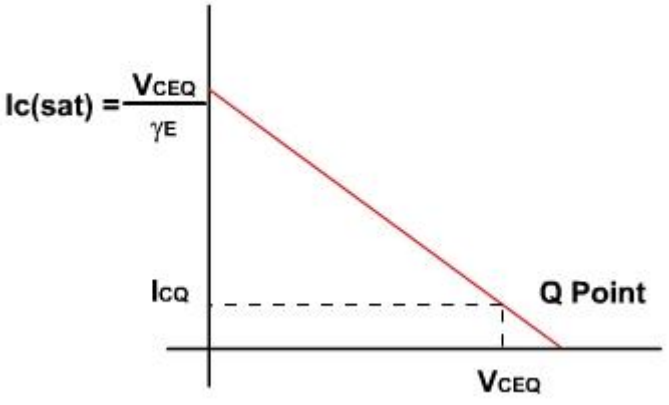

Fig. 2

Class A amplifier introduces non-linear distortion in input wave means elongates one half cycle and compresses one half cycle. This can be reduced by swamping. In this case it can be further reduced because both half cycles are identical in shape, is given by non-linear distortion is much less than class A.

Load power is given by

$$P_L = \frac{V_{PP}^2}{8R_L}$$

Since the ac output compliance equals the peak-to-peak voltage, the maximum load power is

$$P_{L(max)} = \frac{V_{CC}^2}{8R_L}$$

$$= \frac{V_{CEQ}^2}{2R_L}$$

$$\text{Current drain } I_s = I_1 + I_2$$

Where, I_1 = current through biasing resistance. When no signal is present $I_2 = I_{CQ}$ and the current drain is small. But when a signal is present, the current drain increase because the upper collector current becomes large.

If the entire ac load line is used, then the upper transistor has a half sine wave of current through it with a peak value of

$I_{C(sat)} = V_{CEQ} / R_L$

The average value of half sine wave is given by

$$I_2 = \frac{1}{2\pi}\int_0^{\pi}\frac{V_{CEQ}}{R_L}\sin\omega t.d\,\omega t$$
$$= \frac{V_{CEQ}}{R_L} * \frac{1}{\pi}$$
$$= \frac{0.318 V_{CEQ}}{R_L}$$

The dc power is supplied to the circuit is $P_S = V_{CC}$ is under no signal conditions, the dc power is small because the current drain is minimum. But when a signal uses the entire ac load line, the dc power supplied to the circuit reaches a maximum.

Biasing a class B amplifier:

In class B amplifier, two complement any transistors are required. Because of the series connection, each transistor drops half the supply voltage. To avoid cross over distortion, the Q-point slightly above cut off, with the correct V_{BE} somewhere between 0.6 and 0.7.

If there is an increase in V_{BE} by few mV it produces 10 times as much emitter current. Because of this it is difficult to find standard resistors that can produce the correct V_{BE} and it needs an adjustable resistor.

The biasing does not solve thermal instability problem. Because for a given collector current, V_{BE} requirement decreases by 2 mV per degree rise in temperature. The voltage divider produces a stiff drive for each diode. Therefore as the temperature increases, the fixed voltage on each emitter diode forces the collector current to increase and this gives rise to thermal run away. When the temperature increases collector current increases, and this is equivalent to Q-point moving up along the vertical dc load line. As the Q-point moves toward higher collector currents, the temperature of the transistor increases further reducing the required V_{BE} .

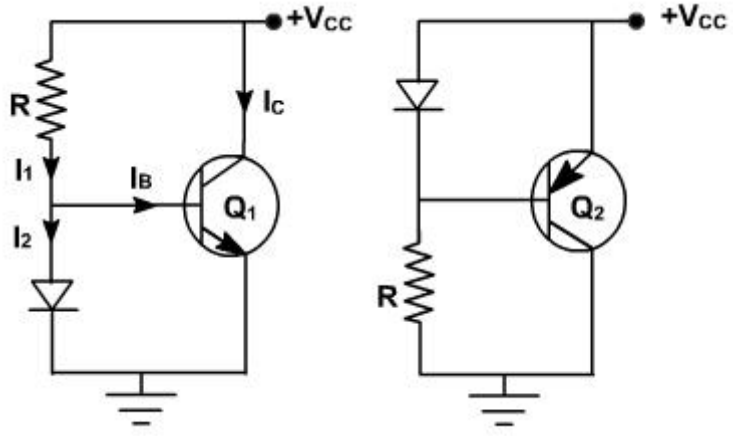

Fig. 3

One way to avoid thermal run away is to use diode bias. It is based on the concept of current mirror as shown in **fig. 3**, the base current is much smaller than the current through the resistor and diode. For this reason, I_1 and I_2 are approximately equal. If the diode curve is identical to the V_{BE} curve of the transistor (V_{BE} , I_E). The diode current equals the emitter and also collector current. Therefore I_1 is nearly equal to I_C.

$I_1 = I_C$.

The collector current is set by controlling the resistor current. This is called a current mirror.

Similarly, pnp transistor can be used as a current mirror. If the V_{BE} curve of the transistor matches the diode curve, the collector equals the resistor current.

Diode bias of class B push pull emitter follower relies on two current mirrors as shown in **fig. 4**.

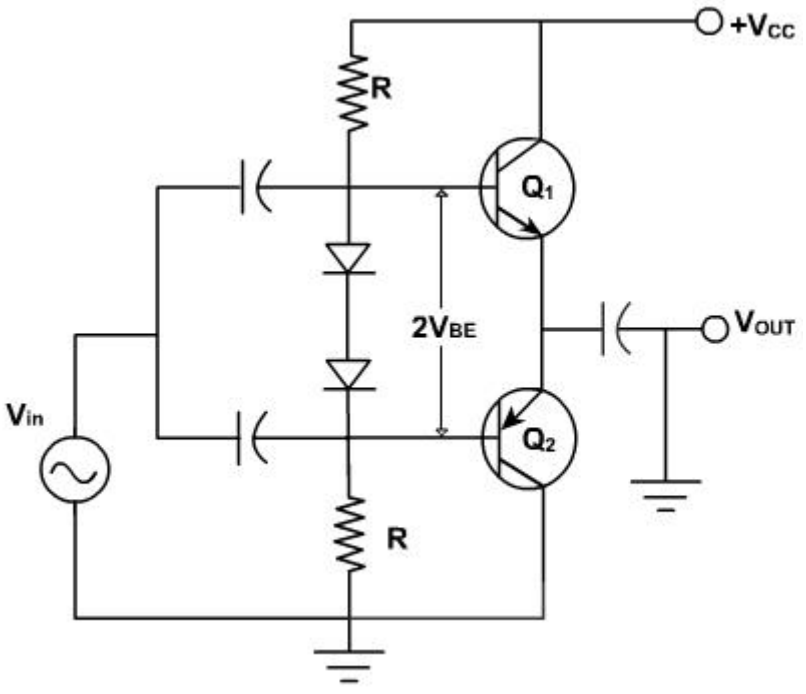

Fig. 4

The upper half is an npn current mirror, and the lower half is a pnp current mirror as shown in **fig. 4**. For diode bias to be immune to changes in temperature, the diode curve must match the V_{BE} curves of the transistor over a wide temperature range. This is easily done in ICs .

Power Calculations for Class B Push-Pull Amplifier

The power delivered by the ac source is split between the transistor and the resistors in the bias circuitry. The ac signal source adds an insignificant additional amunt of power since base currents are small relative to collector currents. Part of the power to the transistor goes to load, and the other part is dissipated by the transistor itself. The following equations specify the various power relationships in the circuit.

The average power supplied by the dc source is

$$P_{VCC} = V_{CC} I_{DC} = V_{CC} \frac{1}{T} \int_0^T i_{cc}(t)dt$$

$i_{CC}(t)$ is the total current and is composed of two components: the dc current through the base bias resistor and diode combination, and the ac collector current through transistor, Q_1. Under quiescent conditions (i.e. zero input) Q_1 is in cutoff mode. Collector current flows during the positive half of the output signal waveform. Therefore we only need to integrate this component of the power supply signal over the first half cycle.

$$I_{C1avg} = \frac{1}{T}\int_0^{T/2} I_{Cmax}\sin\left(\frac{2\pi t}{T}\right)dt = \frac{1}{\pi} I_{C1max}$$

The maximum values of collector current and power delivered to the transistor are

$$I_{Cmax} = \frac{V_{CC}}{2R_{load}}$$

$$P_{VCC}\big|_{Q1,Q2} = \frac{V_{CC} I_{Cmax}}{\pi} = \frac{V_{CC}^2}{2\pi R_{load}}$$

The ac output power, assuming a sinusoidal input, is

$$P_{out}(ac) = \frac{I_{Cmax}^2 R_{load}}{2}$$

The maximum ac output power is found by substituting I_{Cmax} for I_{C1max} to get

$$P_{out}(acmax) = \frac{1}{2}\left(\frac{V_{CC}}{2R_{load}}\right)^2 R_{load} = \frac{V_{CC}^2}{8R_{load}}$$

The total power supplied to the stage is the sum of the power to the transistor and the power to the bias and compensation circuitry.

$$P_{VCC} = \frac{V_{CC}\, I_{Cmax}}{\pi} + \frac{V_{CC}^2}{2R_f + 2R_2}$$

If we subtract the power to the load from the power supplied to the transistors, we find the power being dissipated in the transistors the power dissipated by a single transistor is one half of this value. Thus,

$$P_{transistor} = \frac{1}{2}\left(\frac{V_{CC}\, I_{Cmax}}{\pi} - \frac{I_{Cmax}^2 R_{load}}{2}\right)$$

we are assuming that the base current is negligible. The efficiency of the Class B push-pull amplifier is the ratio of the output power to the power delivered to the transistor. Thus we neglect the power dissipated by the bias circuitry.

$$\eta = \frac{V_{CC}^2 / 8 R_{load}}{V_{CC}^2 / 2\pi R_{load}} = \frac{\pi}{4} = 0.785 \text{ or } 78.5\%$$

This amplifier is more efficient than a Class A amplifier. It is often used in output circuits where efficiency important design requirement.

$$\frac{dP}{dI_{Cmax}} = 0 = \frac{1}{2}\left(\frac{V_{CC}}{\pi} - I_{Cmax}R_{load}\right)$$

$$I_{C1max} = \frac{V_{CC}}{\pi R_{load}}$$

Therefore, $$Pmax = \frac{1}{2}\left(\frac{V_{CC}^2}{\pi^2 R_{load}} - \frac{V_{CC}^2}{2\pi^2 R_{load}}\right) = \frac{V_{CC}^2}{4\pi^2 R_{load}}$$

In choosing a transistor, it is important that the power rating is equal to or exceeds the maximum power P_{max}.

Class C amplifier:

A class C amplifier can produce more power than a class B amplifier.

Consider the case of a radio transmitter in which the audio signals are raised in their frequency to the medium or short wave band to that they can be easily transmitted. The high frequency introduced is in radio frequency range and it serves as the carrier of the audio signal. The process of raising the audio signal to radio frequency called modulation.

The modulated wave has a relatively narrow band of frequencies centered around the carrier frequencies. At any instant, there are several transmitter transmitting programmes simultaneously. The radio receiver selects the signals of desired frequencies to which it is tuned, amplifies it and converts it back to audio range. Therefore, tuned voltage amplifiers are used. In short, the tuned voltage amplifiers selects the desired radio frequency signal out of a number of RF signals present at that instant and then amplifies the selected RF signal to the desired level as shown in **fig. 1**.

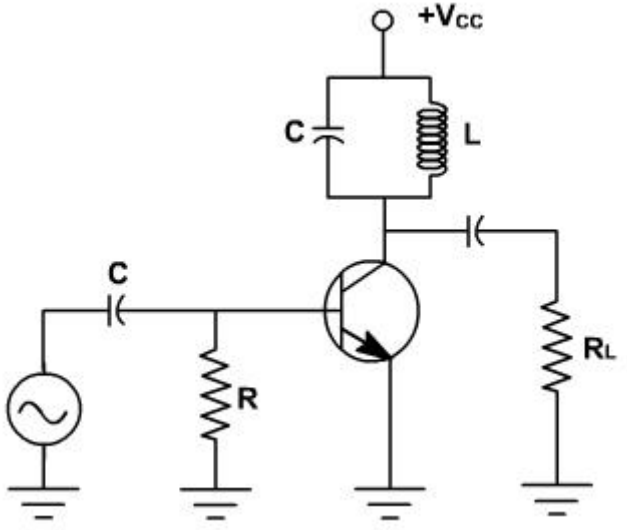

Fig. 1

Class C operation means that the collector current flows for less than 180° of the ac cycle. This implies that the collector current of a class C amplifier is highly non-sinusoidal because current flows in pulses. To avoid distortion, class C amplifier makes use of a resonant tank circuit. This results in a sinusoidal output voltage.

The resonant tank circuit is tuned to the frequency of the input signal. When the circuit has a high quality factor (Q) parallel resonance occurs at approximately

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

At the resonance frequency, the impedence of the parallel resonant circuit is very high as shown in **fig. 2** and is purely resistive. When the circuit is tuned to the resonant frequency, the voltage across R_L is maximum and sinusoidal. The higher the Q of the circuit, the faster the gain drops off on either side of resonance

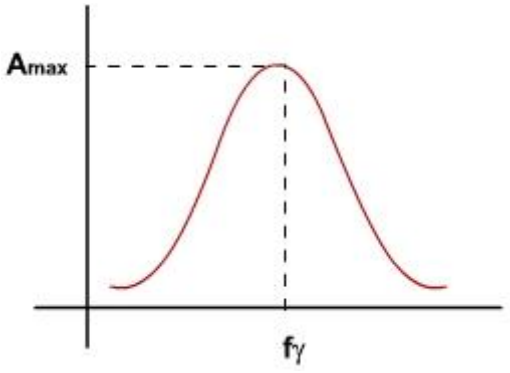

Fig. 2

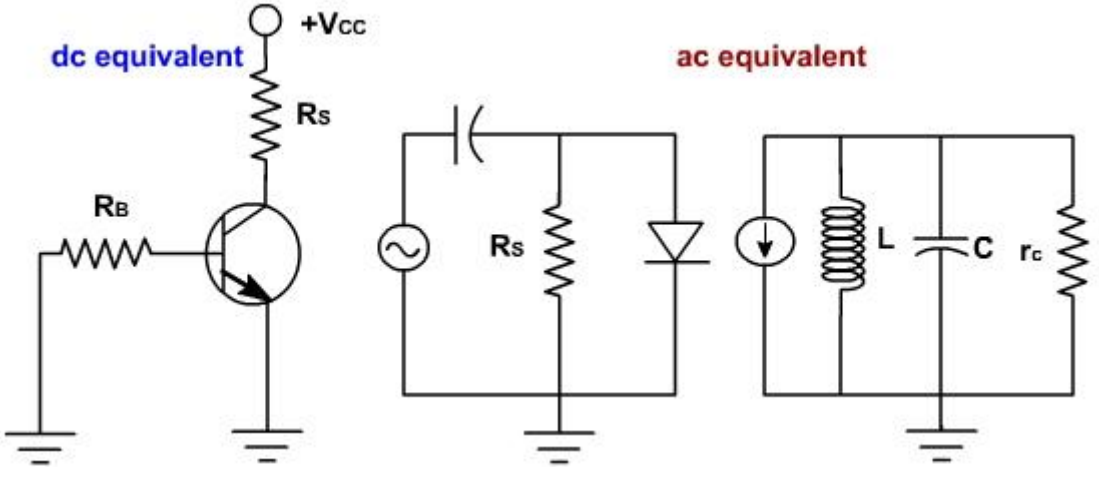

Fig. 3

The dc equivalent circuit is shown **fig. 3**. No bias is applied to the transistor. Therefore, its Q-point is at cut off on the dc load line V_{BE}= 0.7V. Therefore no I_L current flows until input is more than 0.7 V. Also dc resistance is R_S (the resistance of inductor) which is very small and therefore dc load line is almost vertical. There is no danger of thermal runway because there is no current other than from leakage.

The $I_{C(sat)}$ current is given by

$$I_{C(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_C}$$

where r_C is the collector resistance.

The voltage VCE(sate) is given by

$$V_{CE(sat)} = V_{CEQ} + I_{CQ}\, r_C$$

when $I_{CQ} = 0$, $V_{CEQ} = V_{CC}$

$$\therefore I_{C(sat)} = \frac{V_{CC}}{r_C}$$

and $V_{CE(sat)} = V_{CC}$

When the Q of a resonant circuit is greater than 10. One can use the approximate ac equivalent circuit. The series resistance of the inductor is lumped into the collector resistance. At resonance, the peak-to-peak load voltage reaches a maximum. The bandwidth of a resonant circuit is given by

Band width (BW) = f_2 – f_1

f_1 = Lower cut off frequency.

f_2 = Upper cut off frequency

The bandwidth is related to the resonant frequency and the circuit Q as below:

$BW = f_r / Q$

This means a large Q produces small BW equivalent to sharp tuning. These amplifiers have Q greater than 10. This means that the BW is less than 10% of the resonant frequencies. These amplifiers are also called narrow band amplifier.

When the tank circuit is resonant the ac load impedence seen by the collector current source is purely resistive and the collector current is minimum. Above and below resonance, the ac load impedence decreases and the collector current decreases. Any coil or inductor has some series resistance R_S as shown in **fig. 4**.

The Q of all coil is given by.

$Q_L = X_L / R_L$

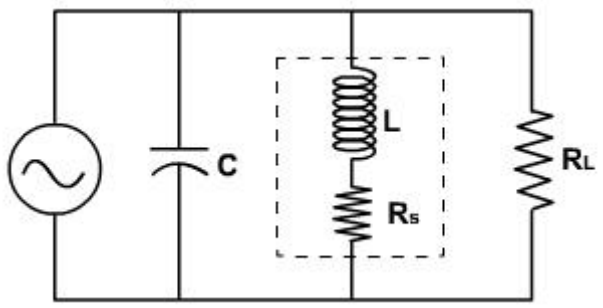

Fig. 4

The series resistance can be replaced by parallel resistance R_P . This equivalent resistance is given by

$R_P = Q_L R_L$

Now all the losses in the coil are now being represented by the parallel resistance R_P and series resistance R_S no longer exists X_C cancels X_L at resonance. Leaving only R_P in parallel with R_L.

Therefore,

$R_C = R_P \parallel R_L$

Q of the overall circuit = r_C / X_L

At the resonance frequency, the impedence of the parallel resonant circuit is very high as shown in **fig. 2** and is purely resistive. When the circuit is tuned to the resonant frequency, the voltage across R_L is maximum and sinusoidal. The higher the Q of the circuit, the faster the gain drops off on either side of resonance

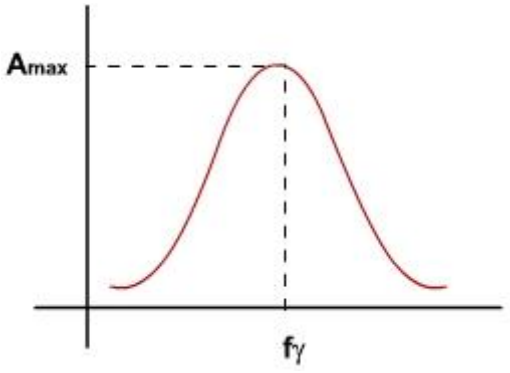

Fig. 2

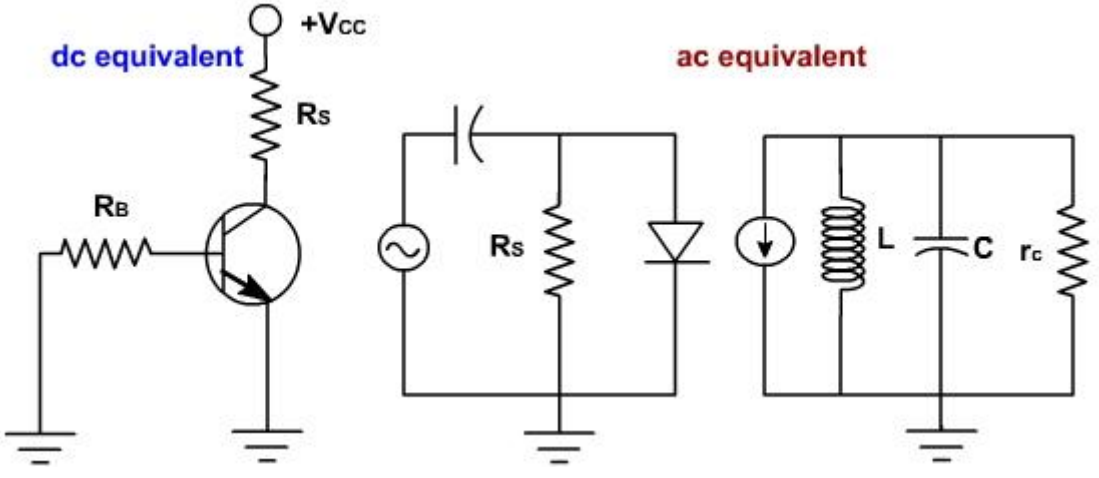

Fig. 3

The dc equivalent circuit is shown **fig. 3**. No bias is applied to the transistor. Therefore, its Q-point is at cut off on the dc load line V_{BE}= 0.7V. Therefore no I_L current flows until input is more than 0.7 V. Also dc resistance is R_S (the resistance of inductor) which is very small and therefore dc load line is almost vertical. There is no danger of thermal runway because there is no current other than from leakage.

The $I_{C(sat)}$ current is given by

$$I_{C(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_C}$$

where r_C is the collector resistance.

The voltage VCE(sate) is given by

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when $I_{CQ} = 0$, $V_{CEQ} = V_{CC}$

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and $V_{CE(sat)} = V_{CC}$

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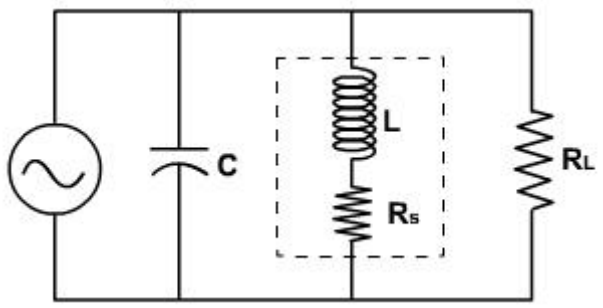


Fig. 4

The series resistance can be replaced by parallel resistance R_P . This equivalent resistance is given by

$R_P = Q_L R_L$

Now all the losses in the coil are now being represented by the parallel resistance R_P and series resistance R_S no longer exists X_C cancels X_L at resonance. Leaving only R_P in parallel with R_L.

Therefore,

$R_C = R_P \parallel R_L$

Q of the overall circuit = r_C / X_L

Current Sources

There are different methods of simulating a dc current source for integrated circuit amplifier biasing. One type of current source used to provide a fixed current is the fixed bias transistor circuit. The problem with this type of current source is that it requires too many resistors to be practically implemented on IC. The resistors in the following circuits are small and easy to fabricate on IC chips. When the current source is used to replace a large resistor the Thevenin resistance of the current source is the equivalent resistance value.

A simple current source

The simple two transistor current source shown in **fig. 1** is commonly used in ICs.

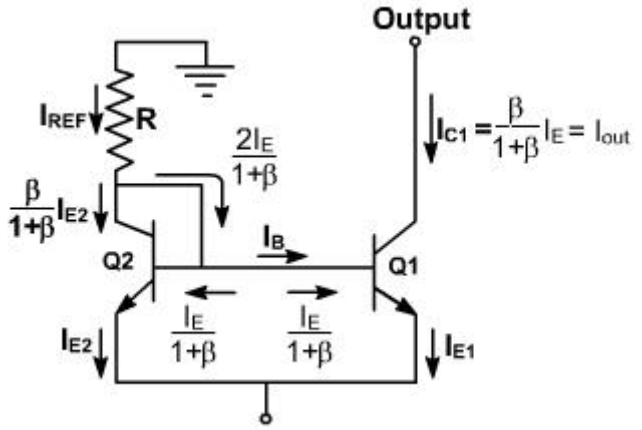


Fig. 1

A reference current is the input to a transistor connected as a diode. The voltage across this transistor drives the second transistor, where $R_E = 0$. Since the circuit has only one resistor, it can be easily fabricated on an IC chip.

The disadvantage of this circuit is that the reference current is approximately equal to the current source. In this circuit, Q_2 is in linear mode, since the collector voltage (output) is higher than the base voltage. The transistor Q_1 and Q_2 are identical devices fabricated on the same IC chip. The emitter currents are equal since the transistors are matched and emitters and bases are in parallel. If we sum the currents of Q_2, we obtain.

$I_B + I_C = I_E$

So $$I_{out} = I_{C1} = I_{E1}\frac{\beta}{1+\beta} = I_{E2}\frac{\beta}{1+\beta}$$

Summing currents at the collector of Q_1 we obtain

$$I_{REF} = \left(\frac{\beta}{1+\beta} + \frac{2}{1+\beta}\right) I_E = \frac{\beta+2}{1+\beta} I_E = I_O$$

If β is large, the current gain is approximately unity and the current mirror has reproduced the input current. One disadvantage of this current source is that its Thevenin resistance (R_{TH}) is limited by the r o ($1 / h_{oe}$) of the transistor. That is

$$R_{TH} = r_o = \frac{V_A}{I_C} \approx \frac{V_A}{I_{REF}}$$

Widlar Current Source

Large resistors are often required to maintain small currents of the order of few μA and these large resistors occupy correspondingly large areas on the IC chip. It is therefore, desirable to replace these large resistors with current sources. One such device is the Widlar current source as shown in **fig. 2**.

The two transistors are assumed perfectly matched. For the base circuit,

$$V_{BE1} - V_{BE2} - I_{E2}R_2 = 0 \qquad \text{(E-4)}$$

For a forward biased base-emitter junction diode, the emitter current is given by

$$i_E = I_0 e^{V_{BE}/nV_T}$$

Since $i_E \approx i_C = I_C$ and n = 1

$$I_C = I_0 e^{V_{BE}/V_T}$$

and $$V_{BE} = V_T \ln\left(\frac{I_C}{I_0}\right) \qquad \text{(E-5)}$$

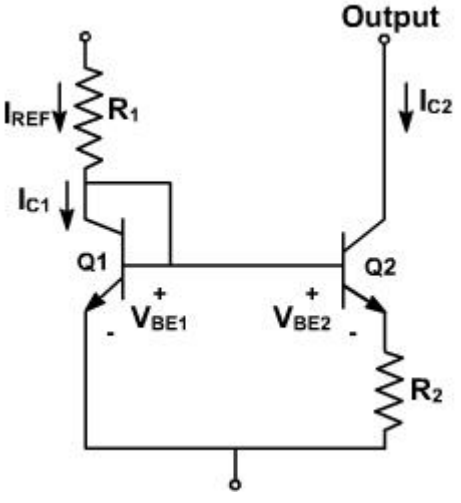


Fig. 2

Substituting V_{BE1} and V_{BE2} from (E-5) to (E-4), we get

$$V_T \ln\left(\frac{I_{C1}}{I_0}\right) - V_T \ln\left(\frac{I_{C2}}{I_0}\right) - I_{E2}R_2 = 0 \qquad \text{(E-6)}$$

We have assumed that both the transistors are matched so that I_{CO}, β and V_T are the same for both the transistors. Thus

$$V_T \ln\left(\frac{I_{C2}}{I_{C1}}\right) = I_{E2}R_2 \approx I_{C2}R_2$$

Hence, $$R_2 = \frac{V_T}{I_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$ (E-7)

where, $$I_{C1} = \frac{V_{CC} - V_{BE}}{R_1}$$ (E-8)

For design purposes, I_{C1} is usually known since it is used as the reference for all current sources on the entire chip and I_{C2} is t he desired output current. The Widlar circuit can also be used to simulate a high resistance.

Example-1

Design a Widlar current source to provide a constant current source of 3 ❖A with V_{CC} = 12V, R_1 = 50 kO, β =100 and V_{BE} = 0.7V

Solution:

The circuit is given in **fig.2** . Applying KVL to the Q_1 transistor we get,

$$I_{C1} = I_{REF} = \frac{12 - 0.7}{5 \times 10^3} = 0.226 \text{ mA}$$

Using the equation (E-7) we can calculate R_2

$$3 \times 10^{-6} R_2 = 0.025 \ln\left(\frac{2.26 \times 10^{-4}}{3 \times 10^{-6}}\right)$$

or $R_2 = 36 \text{ k}\Omega$

Wilson Current Source

Another current source transistor configuration that provides a very large parallel resistance is the Wilson current source which uses three transistors and provides this capability an the output is almost independent of the internal transistor characteristics. The Wilson current source as shown in **fig. 3**, uses the negative feedback provided by Q_3 to raise the output impedance

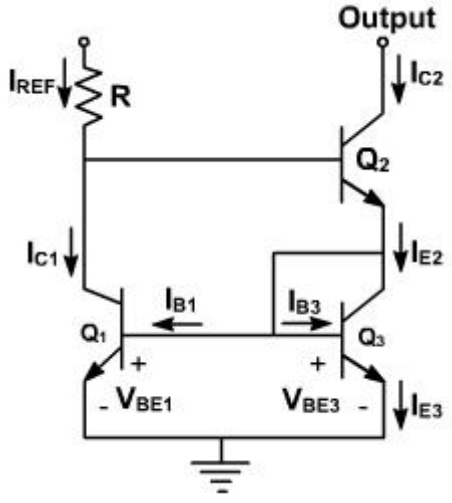


Fig. 3

The difference between the reference current and I_{C1} is the base current of Q_2.

$I_{E2} = (\beta + 1)\, I_{B2} = I_{C3}$ (E-9)

Since the base of Q_1 is connected to the base of Q_3, the currents in Q_1 are approximately independent of the voltage of the collector of Q_2. As such, the collector current of Q_2 remains almost constant providing high output impedance.

Let us now see that I_{C2} is approximately equal to I_{REF}. Applying Kirchhoff's current law at the emitter of Q_2 yields

$I_{E2} = I_{C3} + I_{B3} + I_{B1}$ (E-10)

Using the relationship between collector and base currents

$$I_{E2} = I_{C3}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C1}}{\beta} \qquad \text{(E-11)}$$

Since all three transistors are matched, $V_{BE1} = V_{BE2} = V_{BE3}$ and $\beta_1 = \beta_2 = \beta_3$

With identical transistors, current in the feedback path splits equally between the bases of Q_1 and Q_3 leading so that $I_{B1} = I_{B3}$ and therefore $I_{C1} = I_{C3}$. Thus, the emitter current of Q_2 becomes

$$I_{E2} = I_{C3}\left(1 + \frac{2}{\beta}\right) \quad \text{(E-12)}$$

The collector current of Q_2 is

$$I_{C2} = \frac{I_{E2}\,\beta}{1+\beta} = \frac{I_{C3}\,(1 + 2/\beta)\,\beta}{1+\beta} \quad \text{(E-13)}$$

Solving for I_{C3} yields

$$I_{C3} = \frac{I_{C2}\,(1+\beta)}{\beta\,(1+2/\beta)} = I_{C2}\,\frac{1+\beta}{2+\beta} \quad \text{(E-14)}$$

Summing currents at the base of Q_2,

$$I_{C1} = I_{REF} - \frac{I_{C2}}{\beta} \quad \text{(E-15)}$$

$$I_{C2} = (I_{REF} - I_{C1}) \quad \text{(E-16)}$$

Since $I_{C1} = I_{C3}$, we substitute I_{C3} to obtain

$$I_{C2} = \beta I_{REF} - \frac{\beta\,(1+\beta)}{\beta+2}\,I_{C2} \quad \text{(E-17)}$$

and solving for I_{C2}

$$I_{C2} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}\,I_{REF} = \left[1 - \frac{2}{\beta^2 + 2\beta + 2}\right] I_{REF} \quad \text{(E-18)}$$

Equation (E-10) shows that β has little effect upon I_{C2} since, for reasonable values of β.

$$\frac{2}{\beta^2 + 2\beta + 2} << 1 \quad \text{(E-19)}$$

Therefore, $I_{C2} = I_{REF}$

Multiple Current sources Using Current Mirrors

A number of current sources can be obtained from a single reference voltage. If the current is approximately the same as the reference voltage, the simple current source can be used as shown in **fig. 4** for Q_2 and Q_3.

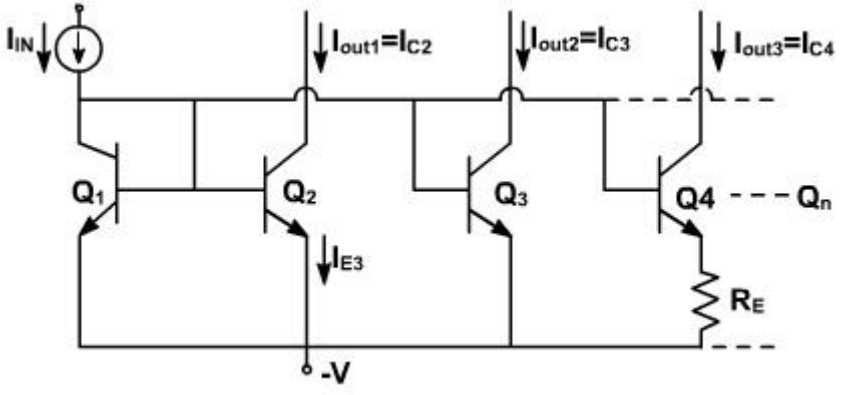


Fig. 4

Notice that Q_4 has an emitter resistance, which makes the current source a Widlar current source. Thus the amount of current delivered by this source can be determined by the size of the emitter resistor. This type of circuit is useful in integrated circuit chips as the one reference circuit can be used to develop current sources throughout the chip. When using the Widlar circuit, the currents can be different from the reference current.

The errors in base current, however, do accumulate when multiple outputs are used and the current gain tends to deviate from unity. In these types of circuits, lateral transistors can be used since it is not important that b be large. Lateral transistors usually have a β of approximately 20 which is more than adequate for current sources.

Example -2:

For the circuit shown in **fig. 5**, determine the emitter current in transistor Q_3. Given that $\beta = 100$, $V_{BE} = 0.715V$.

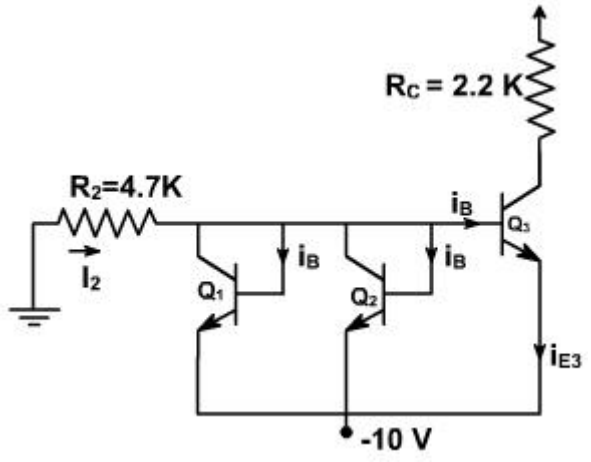


Fig. 5

Solution:

Since all transistor are identical, there V_{BE} voltage drop will be same.

$$\therefore I_2 = \frac{10 - 0.715}{4.7K}$$
$$= 1.976 \text{ mA}$$

Let I_B be the base current of each transistor and I_C be the collector current of Q_1 and Q_2.

Therefore,

$$2I_C + 3I_B = I_2$$
$$2 \times I_B + 3I_B = 1.976 \text{ mA}$$
$$\therefore I_B = 9.73 \text{ A}$$
$$I_E = (1+\beta) I_B$$
$$= 0.983 \text{ mA}$$

Example - 1

Determine the current and voltage gains for the two-stage capacitor-coupled amplifier shown in **fig. 1**.

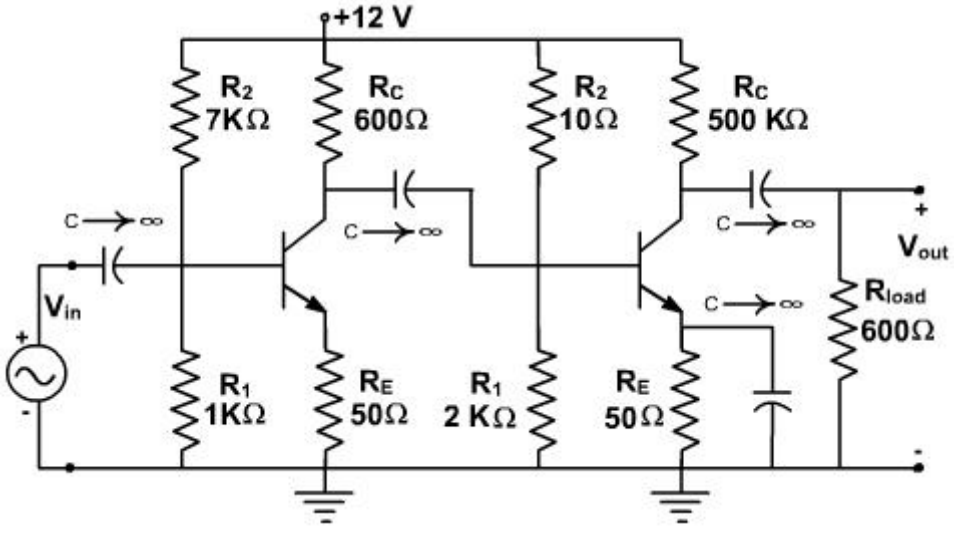


Fig. 1

Solution:

We develop the hybrid equivalent circuit for the multistage amplifier. This equivalent is shown in **fig. 2**. Primed variables denote output stage quantities and unprimed variables denote input stage quantities.

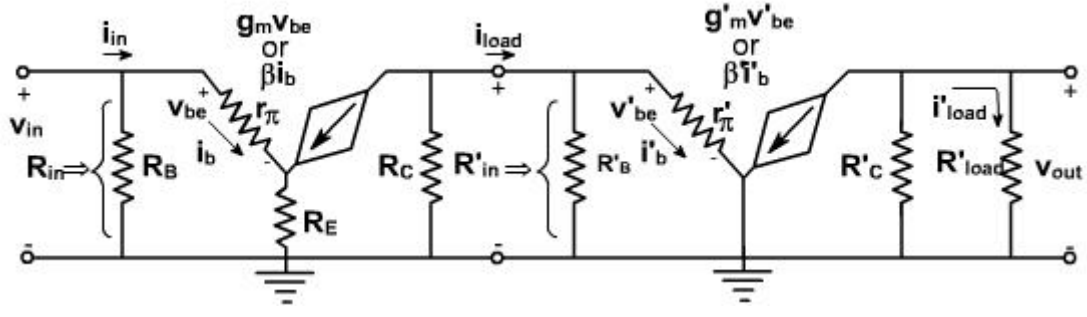


Fig. 2

Calculations for the output stages are as follows

$$R'_B = 10\,K\Omega \parallel 2\,K\Omega = \frac{10^4 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 1.67\,K\Omega$$

$$V'_{BB} = 12V \times \frac{2\,K\Omega}{10\,K\Omega + 2\,K\Omega} = \frac{12 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 2\,V$$

$$I'_{CQ} = \frac{V'_{BB} - V_{BE}}{R'_B/\beta + R'_B} = 22\,mA$$

$$r'_e = \frac{26(mV)}{I_{CQ}} = 1.77\ \ \Omega$$

For the input stage,

$$R_B = 7\,K\Omega \| 1K\Omega = \frac{7000 \times 1000}{7000 + 1000} = 875\,\Omega$$

$$V_{BB} = 12\,\frac{1K\Omega}{1\,K\Omega + 7\,K\Omega} = \frac{12 \times 1000}{700 + 1000} = 1.5\,V$$

$$I_{CQ} = \frac{1.5 - 0.7}{875/200 + 50} = 14.7\ \ mA$$

$$r_e' = \frac{26\ (mV)}{14.7\ (mA)} = 1.77\,\Omega$$

The input resistance is determined as:

$$R_{in} = R_B \| (r_x + \beta R_E) = \frac{875 \times 200 \times (1.77 + 50)}{875 + 10{,}354} = 807\ \Omega$$

The current gain, A_i, can be found by applying the equations derived earlier, where the first stage requires using the correct value for R_{load} derived form the value of R_{in} to the next stage.

Alternatively, we analyze **fig. 2** by extracting four current dividers as shown in **fig. 3**.

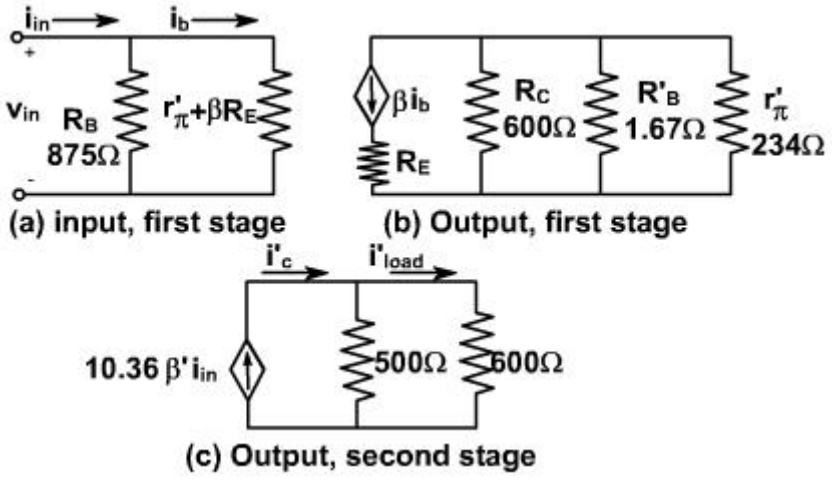


Fig. 3

The current division of the input stage is

$$i_b = \frac{R_B\, i_{in}}{R_B + r_\pi + \beta R_E} = 0.078\ i_{in}$$

The output of the first stage is coupled to the input of he second stage in **fig. 3(b)**. The input resistance of the second stage is

$$R'_{in} = R'_B \parallel r'_\pi = 205\ \Omega$$

The current in R'_{in} is i_{load} and is given by

$$i_{load} = \frac{15.6\, i_{in} \times 600}{805} = 11.6\, i_{in}$$

Again, i_{load} is current-divided at the input to the second stage. Thus,

$$i'_b = \frac{-R'_B\, i_{load}}{R'_B + r'_\pi} = -10.2\, i_{in}$$

The output current is found from **fig. 3(c)**:

$$i'_{load} = \frac{10.2\, i_{in} \times 200 \times 500}{500 + 600} = 927\ .\ i_{in}$$

The current gain is then

A_i =927

Now using the gain impedance formula, we find the voltage gain:

$$A_v = \frac{927 \times 600}{807} = 689$$

Impedance Coupling:

At higher frequency impedance coupling is used. The collector resistance is replaced by an inductor as shown in **fig. 4**. As the frequency increases, X_L approaches infinity and each inductor appears open. In other words, inductors pass dc but block ac. When used in this way, the inductors are called RFchokes.

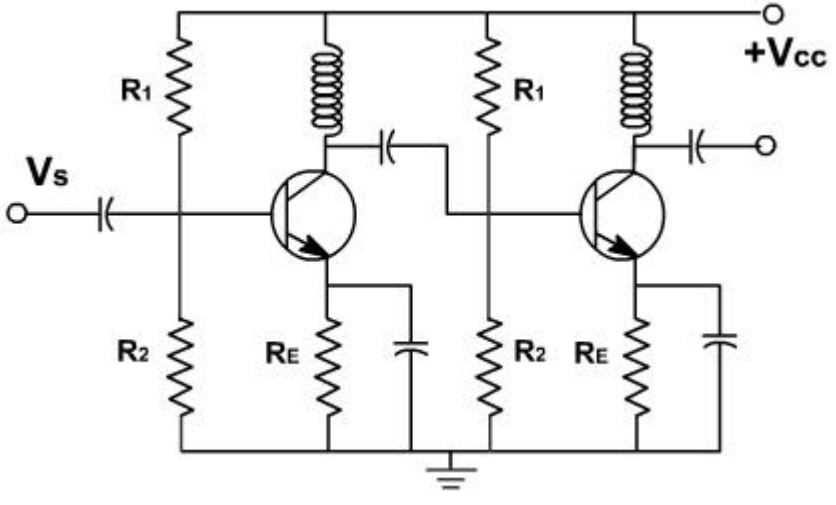


Fig. 4

The advantage is that no signal power is wasted in collector resistors. These RF chokes are relatively expensive and their impedance drops off at lower frequencies. It is suitable at radio frequency above 20 KHz.

Transformer Coupling:

In this case a transformer is used to transfer the ac output voltage of the first stage to the input of the second stage. **Fig. 5**, the resistors R_C is replaced by the primary winding of the

transformer. The secondary winding is used to give input to next stage. There is no coupling capacitor. The dc isolation between the two stages provided by the transformer itself. There is no power loss in primary winding because of low resistance.

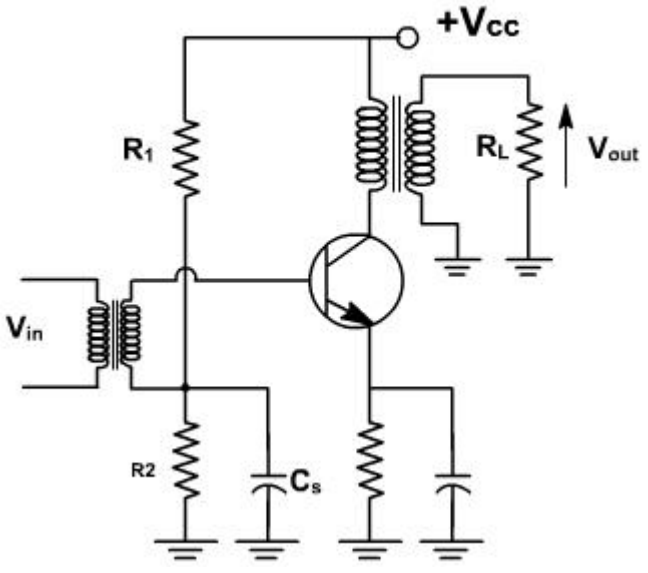


Fig. 5

At low frequency the size and cost of the transformer increases. Transformer coupling is still used in RF amplifiers. In AM radio receivers, RF signal have frequencies 550 to 1600 KHz. In TV receivers, the frequencies are 54 to 216 MHz. At these frequency the size and cost of the transformer reduces. C_S capacitor is used to make other point of transformer grounded, so that ac signal is applied between base and ground.

Tuned Transformer Coupling:

In this case a capacitor is shunted across primary winding to get resonance as shown in **fig. 6**. At this frequency the gain is maximum and at other frequencies the gain reduces very much. This allows us to filter out all frequencies except the resonant frequency and those near it. This is the principle behind tuning in a radio station or TV channel.

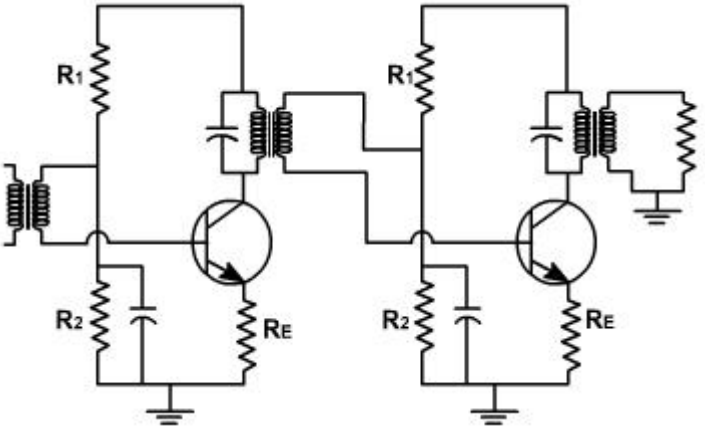


Fig. 6

Example - 2

Design a transformer-coupled amplifier as shown in **fig. 7** for a current gain of $A_i = 80$. Find the power supplied to the load and the power required from the supply.

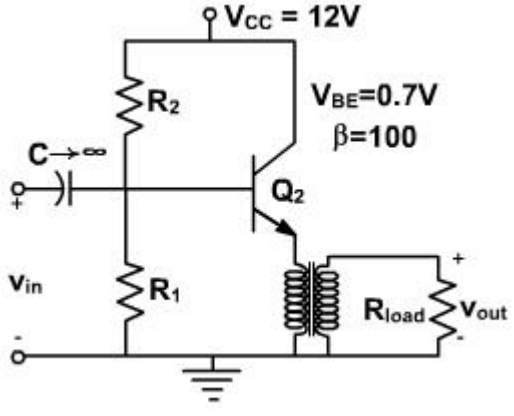


Fig. 7

Solution:

We first use the design equation to find the location of the Q-point for maximum output swing.

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{12}{a^2 R_{load}} = 23.4\text{mA}$$

Since the problem statement requires a current gain of 80, the amplifier must have a current gain of 10 because the transformer provides an additional gain of 8. We use the equations from Chapter 5 to find the base resistance R_B,

$$A_i = \frac{R_B}{R_B/\beta + r_e + R_E} = 10$$

where

$$R_E = a^2 R_{load} = 512\ \Omega$$

We note that r_e is sufficiently small to be neglected. Then, solving for R_B yields

$$R_B = 54.69\ K\Omega$$

$$V_{BB} = \frac{I_{CQ}R_B}{\beta} + V_{BE} = 2.03\ V$$

Now solving for the bias resistors,

$$R_1 = \frac{R_B}{1 + V_{BB}/V_{CC}} = 6.85\ K\Omega$$

$$R_2 = \frac{V_{CC}R_B}{V_{BB}} = 33.6\ K\Omega$$

The design is now complete. The power delivered by the source is given by

$$P_{V_{cc}} = V_{CC}I_{CQ} + \frac{V_{CC}^2}{R_1 + R_2} = 284\ mW$$

The power dissipated in the load is

$$P_{load} = \frac{(0.9a\, I_{CQ})^2\, R_{load}}{2} = 114\ \ mW$$

We have restricted operation to the linear region by eliminating 5% of the maximum swing near cutoff and saturation. The efficiency is the ratio of the load to source power.

$$\eta = \frac{114}{284} = 0.4 \text{ or } 40\ \%$$

Oscillators

Objectives:

– To understand

• The basic operation of an Oscillator • the working of low frequency oscillators

– RC phase shift oscillator – Wien bridge Oscillator

• the working of tuned oscillator – Colpitt's Oscillator, Hartley Oscillator – Crystal Oscillator

• the working of UJT Oscillator

Basic operation of an Oscillator

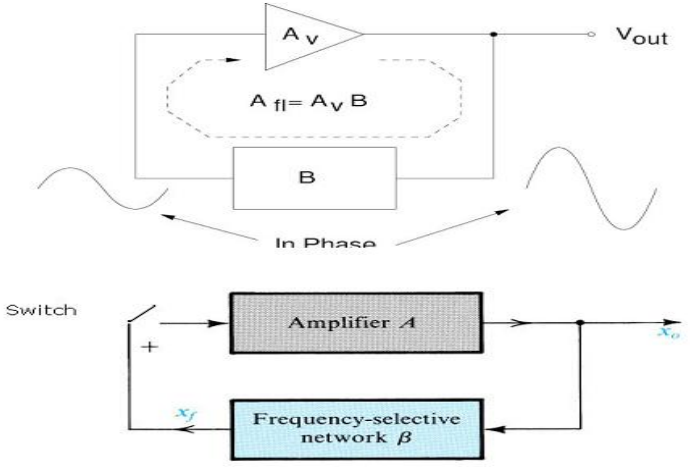
• An amplifier with positive feedback results in oscillations if the following conditions are satisfied:

– The loop gain (product of the gain of the amplifier and the gain of the feedback network) is unity

– The total phase shift in the loop is 0□

• If the output signal is sinusoidal, such a circuit is referred to as sinusoidal oscillator.

When the switch at the amplifier input is open, there are no oscillations. Imagine that a voltage Vi is fed to the circuit and the switch is closed. This results in V



When the switch at the amplifier input is open, there are no oscillations. Imagine that a voltage Vi is fed to the circuit and the switch is closed. This results in $V_o = A_V V_i$ and $\beta V_o = V_f$ is fed back to the circuit. If we make Vf = V then even if we remove the input voltage to the circuit, the output continues to exist.

$V_o = A_V V_i$

$\beta V_o = V_f$

$\beta A_V V_i = V_f$

If V_f has to be same as V_i, then from the above equation, it is clear that, □ A =1V

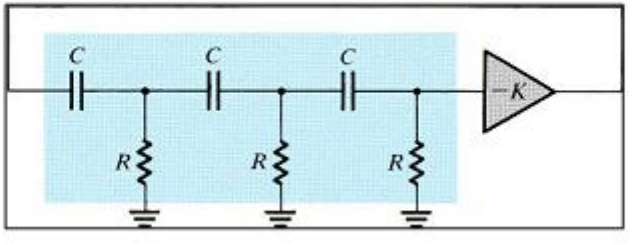
Thus in the above block diagram, by closing the switch and removing the input, we are able to get the oscillations at the output if □ AV =1, where □ A is called the **Loop gain**.

Positive feedback refers to the fact that the fed back signal is in phase with the input signal. This means that the signal experiences 0□ phase shift while traveling in the loop. The above condition along with the unity loop gain needs to be satisfied to get the sustained oscillations. These conditions are referred to as 'Barkhausen criterion'. Another way of seeing how the feedback circuit provides operation as an oscillator is obtained by noting the denominator in the basic equation

Af = A / (1+□ A).

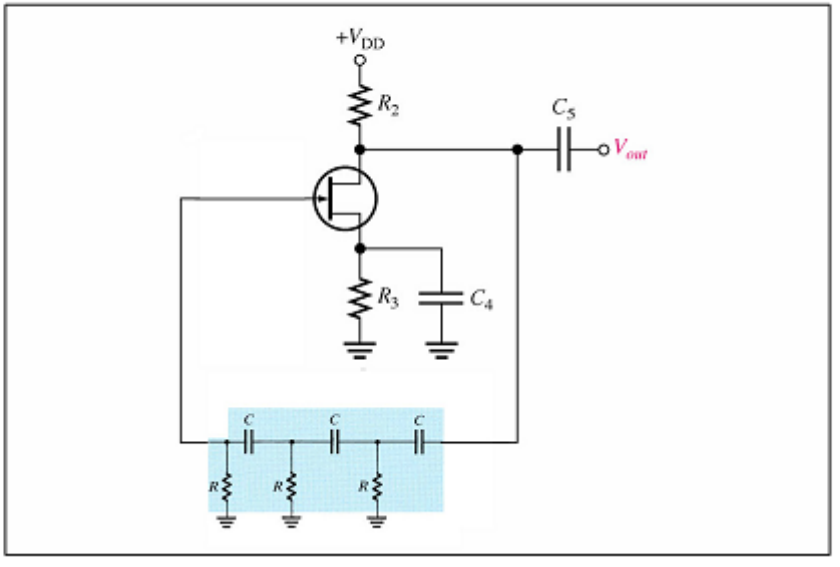
When □ A =-1 or magnitude 1 at a phase angle of 180□ , the denominator becomes 0 and the gain with feedback Af becomes infinite.Thus, an infinitesimal signal (noise voltage) can provide a measurable output voltage, and the circuit acts as an oscillator even without an input signal.

Phase shift oscillator



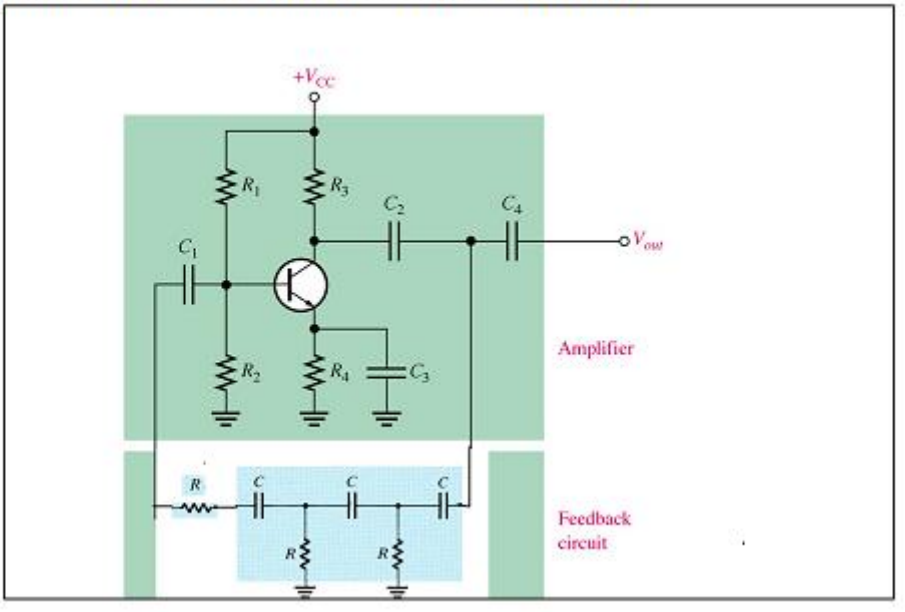
- The phase shift oscillator utilizes three RC circuits to provide 180º phase shift that when coupled with the 180º of the op-amp itself provides the necessary feedback to sustain oscillations.
- The gain must be at least 29 to maintain the oscillations. The frequency of resonance for the this type is similar to any RC circuit oscillator: $f_r = 1/2\sqrt{\pi 6}RC$

FET phase shift oscillator



- The amplifier stage is self biased with a capacitor bypassed source resistor Rs and a drain bias resistor Rd . The FET device parameters of interest are gm and rd.
- $|A| = g_m R_L$, where $R_L = (R_D r_d / R_D + r_d)$
- At the operating frequency, we can assume that the input impedance of the amplifier is infinite .
- This is a valid approximation provided, the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected.
- The output impedance of the amplifier stage given by R should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs.

RC Phase shift Oscillator - BJT version



• If a transistor is used as the active element of the amplifier stage, the output of thfeedback network is loaded appreciably by the relatively low input resistance (h ie) of the transistor.

• An emitter – follower input stage followed by a common emitter amplifier stage could be used.If a single transistor stage is desired, the use of voltage – shunt feedback is more suitable. Here, the feedback signal is coupled through the feedback resistor R' in series with the amplifier stage input resistance (R i).

$$f = (1/2\pi RC)[1/\sqrt{6 + 4(RC / R)}]$$

$$h_{fe} > 23 + 29\,(R/RC) + 4\,(RC / R)$$

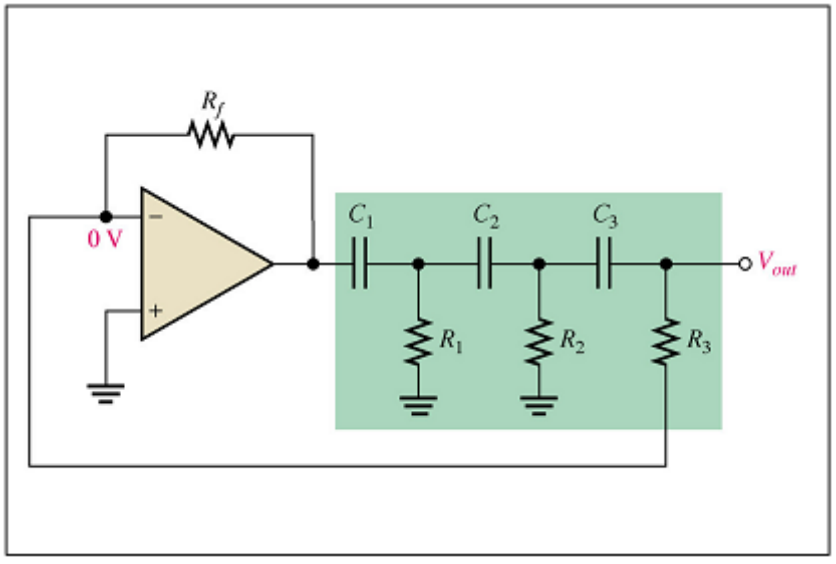
Problem:

It is desired to design a phase shift oscillator using an FET having g = 5000 □ S rd= 40 k□ , and a feedback circuit value of R = 10 k□ . Select the value of C for oscillator operation at 5 kHz and RD for A > 29 to ensure oscillator action.

Solution:

- $f = 1/2\sqrt{6}RC$; $C = 1/2\sqrt{6}Rf = 1.3nF$
- $|A| = g_m R_L$

  $Let\ A = 40;\ RL = |A| / gm = 8\ k\Omega$



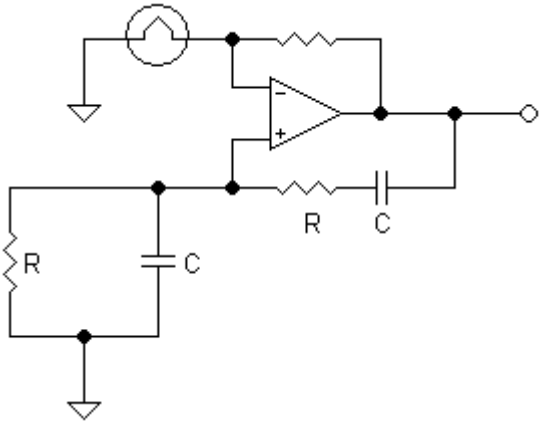
Wien bridge oscillator

A **Wien bridge oscillator** is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The circuit is based on an electrical network originally developed by Max Wien in 1891. The bridge comprises four resistors and two capacitors. It can also be viewed as a positive feedback system combined with a bandpass filter. Wien did not have a means of developing electronic gain so a workable oscillator could not be realized.

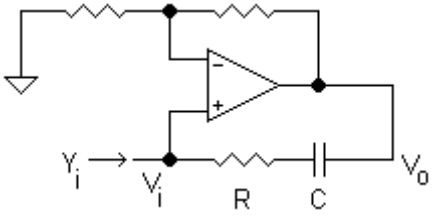
The modern circuit is derived from William Hewlett's 1939 Stanford University master's degree thesis. Hewlett, along with David Packard co-founded Hewlett-Packard. Their first product was the HP 200A, a precision sine wave oscillator based on the Wien bridge. The 200A was one of the first instruments to produce such low distortion.

The frequency of oscillation is given by:

$$f = \frac{1}{2\pi RC}$$



Analysis



Input admittance analysis

If a voltage source is applied directly to the input of an **ideal** amplifier with feedback, the input current will be:

$$i_{in} = \frac{v_{in} - v_{out}}{Z_f}$$

Where v_{in} is the input voltage, v_{out} is the output voltage, and Z_f is the feedback impedance. If the voltage gain of the amplifier is defined as:

$$A_v = \frac{v_{out}}{v_{in}}$$

And the input admittance is defined as:

$$Y_i = \frac{i_{in}}{v_{in}}$$

Input admittance can be rewritten as:

$$Y_i = \frac{1 - A_v}{Z_f}$$

For the Wien bridge, Z_f is given by:

$$Z_f = R + \frac{1}{j\omega C}$$

$$Y_i = \frac{(1 - A_v)\left(\omega^2 C^2 R + j\omega C\right)}{1 + (\omega C R)^2}$$

If A_v is greater than 1, the input admittance is a negative resistance in parallel with an inductance. The inductance is:

$$L_{in} = \frac{\omega^2 C^2 R^2 + 1}{\omega^2 C\left(A_v - 1\right)}$$

If a capacitor with the same value of C is placed in parallel with the input, the circuit has a natural resonance at:

$$\omega = \frac{1}{\sqrt{L_{in} C}}$$

Substituting and solving for inductance yields:

$$L_{in} = \frac{R^2 C}{A_v - 2}$$

If A_v is chosen to be 3:

$L_{in} = R^2 C$

Substituting this value yields:

$$\omega = \frac{1}{RC}$$

Or:

$$f = \frac{1}{2\pi RC}$$

Similarly, the input resistance at the frequency above is:

$$R_{in} = \frac{-2R}{A_v - 1}$$

For $A_v = 3$:

$R_{in} = -R$

If a resistor is placed in parallel with the amplifier input, it will cancel some of the negative resistance. If the net resistance is negative, amplitude will grow until clipping occurs. Similarly, if the net resistance is positive, oscillation amplitude will decay. If a resistance is added in parallel with exactly the value of *R*, the net resistance will be infinite and the circuit can sustain stable oscillation at any amplitude allowed by the amplifier.

Notice that increasing the gain makes the net resistance more negative, which increases amplitude. If gain is reduced to exactly 3 when a suitable amplitude is reached, stable, low distortion oscillations will result. Amplitude stabilization circuits typically increase gain until a suitable output amplitude is reached. As long as *R*, *C*, and the amplifier are linear, distortion will be minimal.

Crystal oscillator

A **crystal oscillator** is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. The most common type of piezoelectric resonator used is the quartz crystal, so oscillator circuits designed around them were called "crystal oscillators".

Quartz crystals are manufactured for frequencies from a few tens of kilohertz to tens of megahertz. More than two billion (2×10^9) crystals are manufactured annually. Most are small devices for consumer devices such as wristwatches, clocks, radios, computers, and cellphones. Quartz crystals are also found inside test and measurement equipment, such as counters, signal generators, and oscilloscopes

A quartz crystal can be modeled as an electrical network with a low impedance (series) and a high impedance (parallel) resonance point spaced closely together. Mathematically (using the Laplace transform) the impedance of this network can be written as:

$$Z(s) = \left(\frac{1}{s \cdot C_1} + s \cdot L_1 + R_1\right) || \left(\frac{1}{s \cdot C_0}\right)$$

or,

$$Z(s) = \frac{s^2 + s\frac{R_1}{L_1} + {\omega_s}^2}{(s \cdot C_0)[s^2 + s\frac{R_1}{L_1} + {\omega_p}^2]}$$

$$\Rightarrow \omega_s = \frac{1}{\sqrt{L_1 \cdot C_1}}, \quad \omega_p = \sqrt{\frac{C_1 + C_0}{L_1 \cdot C_1 \cdot C_0}} = \omega_s\sqrt{1 + \frac{C_1}{C_0}} \approx \omega_s\left(1 + \frac{C_1}{2C_0}\right) \quad (C_0 \gg$$

where s is the complex frequency ($s = j\omega$), ω_s is the series resonant frequency in radians per second and ω_p is the parallel resonant frequency in radians per second.

Adding additional capacitance across a crystal will cause the parallel resonance to shift downward. This can be used to adjust the frequency at which a crystal oscillator oscillates. Crystal manufacturers normally cut and trim their crystals to have a specified resonance frequency with a known 'load' capacitance added to the crystal. For example, a 6 pF 32 kHz crystal has a parallel resonance frequency of 32,768 Hz when a 6.0 pF capacitor is placed across the crystal. Without this capacitance, the resonance frequency is higher than 32,768 Hz.