Module - 2

FET and SCR:

Introduction JFET:

Construction & operation, JFET Drain characteristics and parameters, JEFT Transfer Characteristic. Square law expression for I_D, Input resistance MOSFET: Depletion and Enhancement type MOSFET - Construction, operation, characteristics & Symbols, refer 7.1, 7.2 7.4 7.5 of Text 2)
CMOS (4.5 of Text 1)

Silicon Controlled Rectifier (SCR).

Two - transistor Model
Switching action, characteristics
phase Control application.
[refer 3.4 upto 3.4.5 of Text 1]

RBT Levels: L1 L2 & L3.

JFET — Junction Field Effect Transistor.

Introduction :-

Field Effect Transistor (FET) are unipolar devices because, they operate only with one type of charge carrier, But Bipolar junction Transistor (BJT) are bipolar devices are uses both electron & hole current.

FET's.

JFET MOSFET

JFET — Junction field effect transistor
MOSFET — metal oxide semiconductor FET.

Field effect is a term which relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminal (gate).

BJT is a current-Controlled device; i.e the base current Controls the amount of collector current.

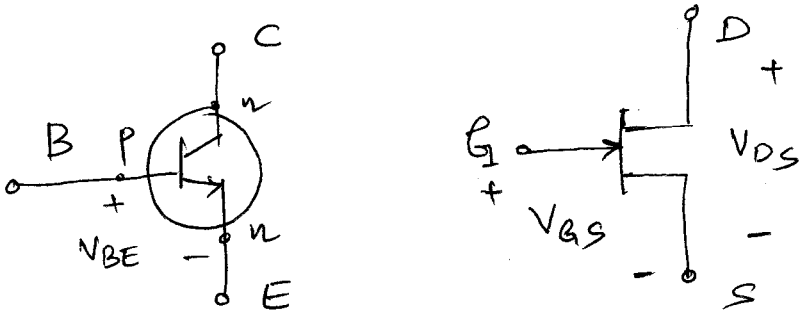
FET is a voltage-Controlled device, where the voltage between two of the terminal (gate and source) Controls the current through the device.

The BJT has few disadvantages such as it offers low input impedances & considerable noise level.

A major advantage of FET's is their very high input resistance. They are non-linear in nature, not widely used as amplifiers. but used where high input impedance is required.

- FETs used in Low-voltage switching applications because they are generally faster than BJT's when turned ON and OFF. IGBT used in high-voltage switching application.

JEFT:- It is a three terminal unipolar semiconductor device in which current conduction is by one type of carrier either electrons or holes. It is a voltage controlled device.



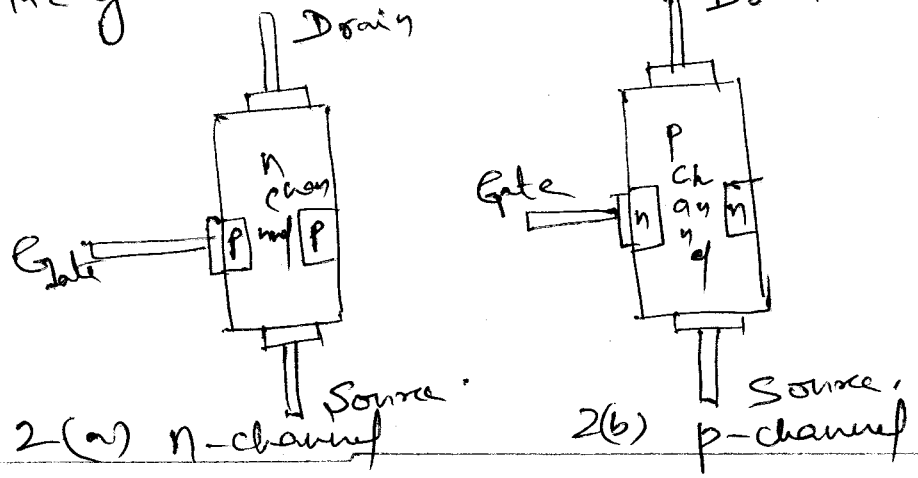
ⓐ BJT (npn).
Control current I_B
Control output I_C

ⓑ n-channel JFET
input voltage V_{GS}
controls output
current.

Basic structure:

Figure shows the basic structures of an n-channel and p-channel JFET are shown in fig. 2 (a) & 2 (b)

In n channel JFET wire leads are connected to each end of the n-channel; the drain is at the upper end, and the source is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the gate lead. gate is connected to p-region.



2(a) n-channel
2(b) p-channel

Fig (2) Basic structure of n-channel & p channel JFET.

Basic operation:

→ Fig (3) shows Applying DC bias voltages applied to an n channel device.

→ V_{DD} provides a drain-to-source voltage and supplies current from drain to source.

→ V_{GG} sets the reverse bias voltage between the gate and the source.

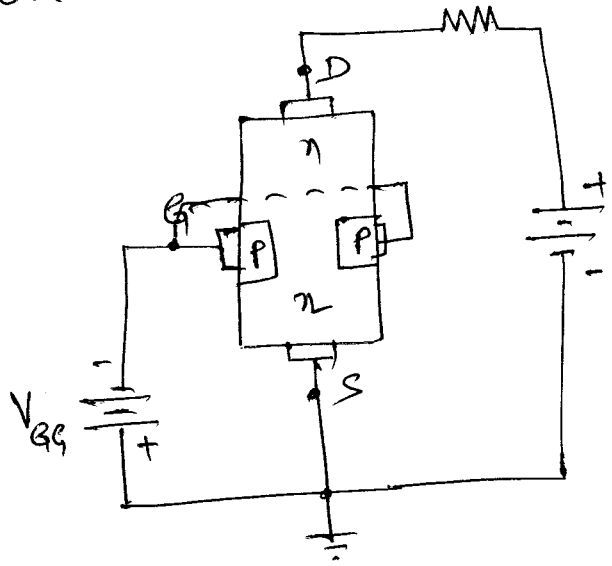


Fig (3).
A biased n-channel JFET

The JFET is always operated with the gate-source pn junction reverse-biased.

Reverse biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn-junction, which extends into the n-channel and thus increases its resistance by restricting the channel width.

The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current I_D.

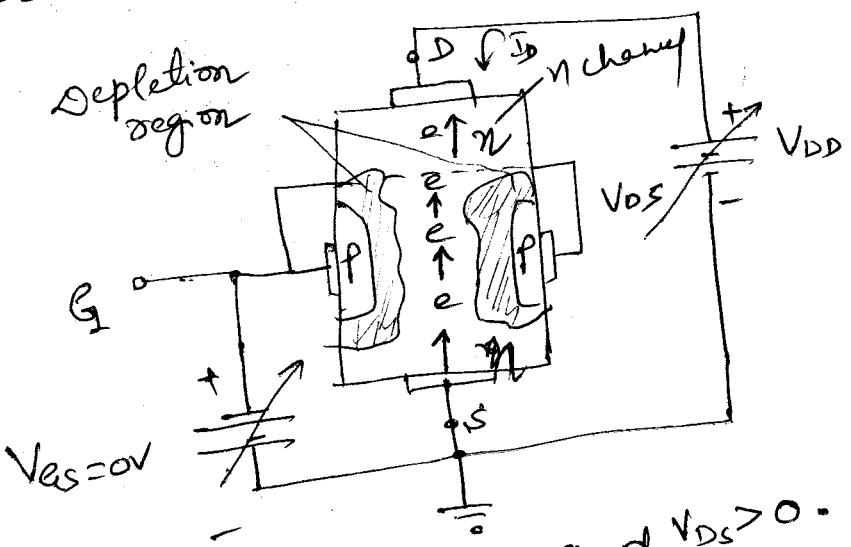
Case (1)

When $V_{GS}=0$, and V_{DS} is increased from zero. Under this condition voltage on the gate terminal is made zero and voltage between drain and source is applied as shown in figure.

The electrons (majority charge carriers) will start flowing from source to drain whereas conventional drain current I_D flows through the channel from drain to source.

The width defines the amount of electrons, flowing through channel. Since $V_{GS}=0$, we cannot control the flow of electrons from source to drain.

The electrons are drawn to the drain terminal establishing the conventional current I_D due to a small V_{DS} applied across drain-source terminals.



JFET at $V_{GS}=0$ V and $V_{DS}>0$.

Case (2): When V_{GS} is applied ($V_{GS}<0$).

When a reverse voltage V_{GS} is applied between gate and source. The reverse bias voltage across the gate source junction is increased.

As a result of this, the depletion regions are widened. Automatically this reduces the width of the conduction channel.

When the gate to source voltage V_{GS} is increased further, a stage is reached at which two depletion regions touch each other as shown in figure.

At this stage, the channel is completely blocked for the flow of electrons from source to drain and hence drain current becomes zero. The value of V_{GS} where $I_D = 0$ referred to as pinch off voltage V_p or $V_{GS(off)}$.

Note: From above explanation, it is clear that current from drain to source can be controlled by the application of potential on gate voltage. For this reason the device is called field effect (voltage controlled) transistor.

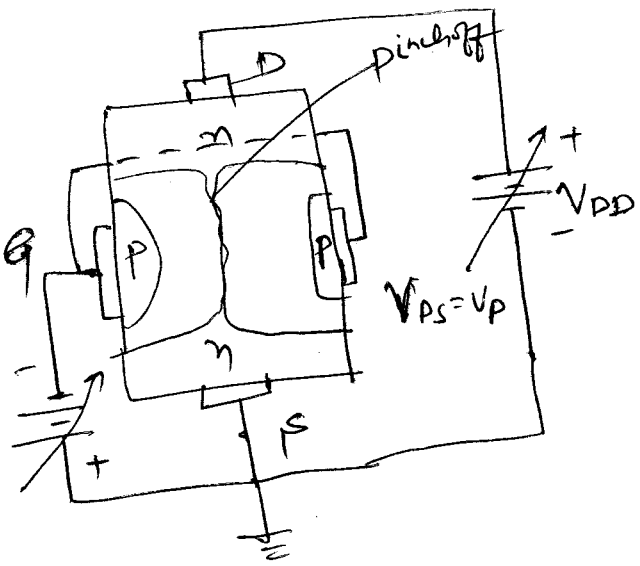


Fig. Pinch-off ($V_{GS} = 0V$, $V_{DS} = V_p$).

$V_{GS} < 0V$: V_{GS} is negative, i.e the gate terminal is made more negative than source. The level of V_{GS} that results in $I_D = 0mA$ is defined by $V_{GS} = V_p$, with V_p being negative voltage for n-channel devices

and a positive voltage for p-channel JFETs.

p-Channel Devices :-

The p-channel JFET is shown in figure is constructed in exactly the same manner as the n-channel device but with a reversal of the p- and n-type materials. The defined current directions and actual polarities of the voltages V_{GS} and V_{DS} are reversed.

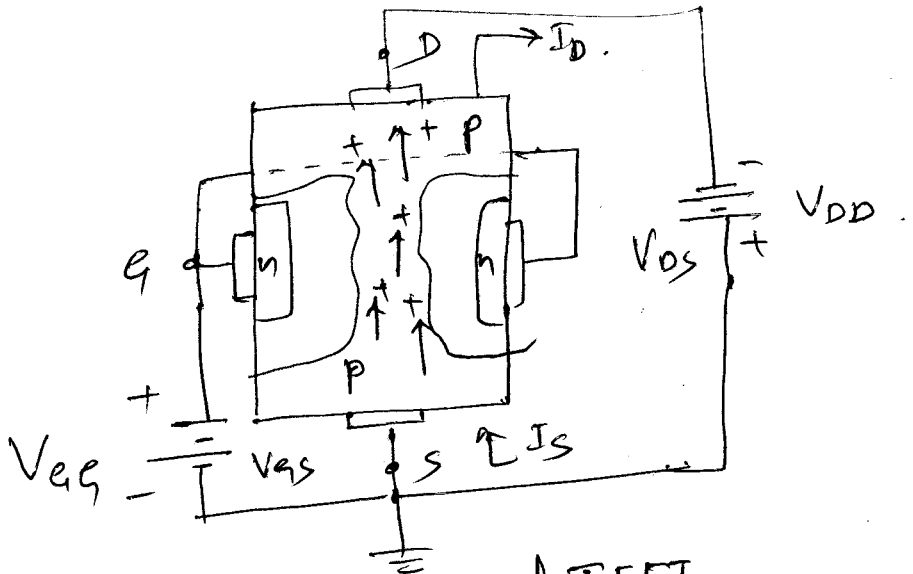
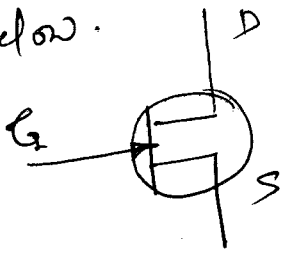


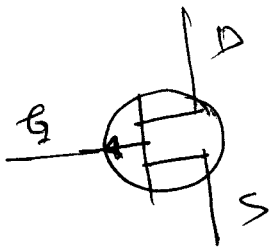
Fig. p-channel JFET.

JFET Symbols.

The ARROWS on the Gate point "in" for n channel JFET and "out" for p channel JFET are shown in figure below.



n-channel JFET



p-channel JFET.

Schematic Symbol.

JFET characteristics and parameters :-

JFET operates as a voltage Controlled, Constant Current device. There are two types of characteristic curve.

(1) Drain characteristics or V-I characteristics.

(2) Transfer characteristics

The set of curves which relate device current and voltage are known as characteristic curves.

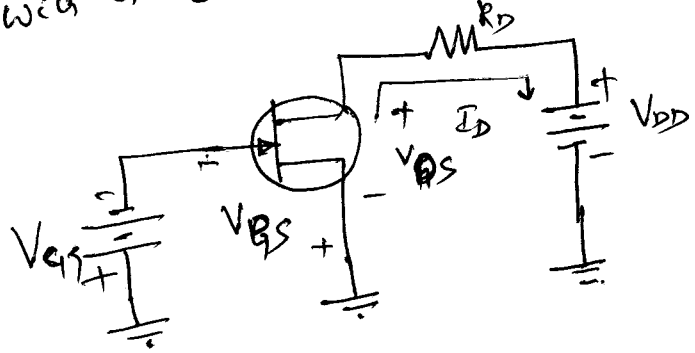
Drain characteristics :-

These curves give relationship between the drain current (I_D) and drain to source voltage (V_{DS}) for different value of gate-to-source voltage (V_{GS}).

Transfer characteristics :-

These curves give relationship between drain current (I_D) and gate to source voltage (V_{GS}) for constant, small positive potential (V_{DS}) applied to the drain to source terminal.

Here the n-channel JFET is Connected in Common source mode. Here we can use potentiometer to vary the voltages V_{GS} and V_{DS}. The voltages V_{DS} and V_{GS} may be measured by the voltmeters connected across the JFET terminals. The I_D can be measured by the milliammeter connected in series with the JFET and supply voltage V_{DD}.



JFET in Common source mode.

JFET Drain characteristics :-

The characteristics of JFET divided into three different regions, namely

(1) Ohmic region
(2) Saturation region.
(3) cut-off region

The voltage applied to the drain is termed as V_{DS} and the voltage to the gate is called as V_{GS}.

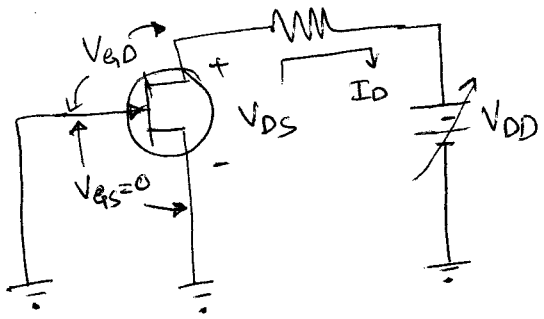
Drain characteristic is also called as output characteristics. Variation of output current I_D by varying the output voltage V_{DS} by keeping input voltage V_{GS} constant.

The circuit arrangement for Drain characteristics is shown in figure.

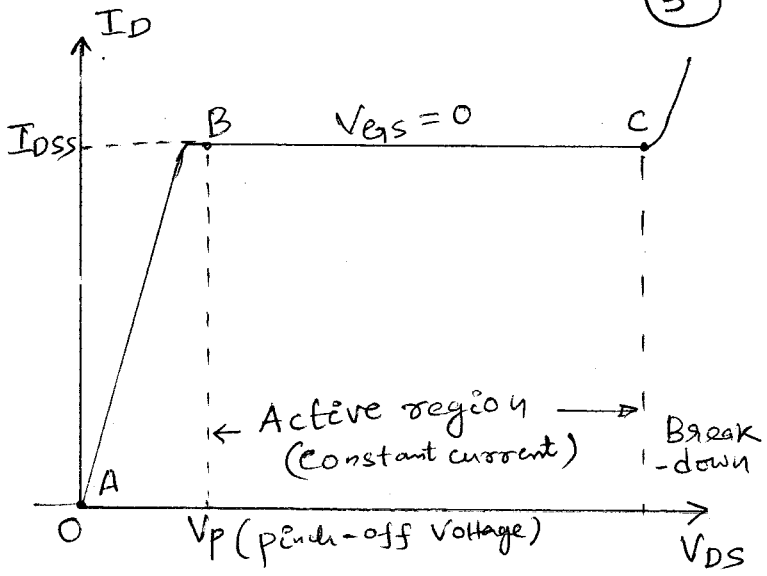
Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0V$). As V_{DD} (and thus V_{DS}) is increased from 0V, I_D will increase proportionally, as shown in figure. (b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ohmic region because V_{DS} and I_D are related by ohm's law.

Ohmic region :- ($V_{DS} > 0$ and $V_{DS} < V_P$).

- Here channel depletion layer is very small and the JFET acts as a variable resistor.
- From point A to B, the drain current increases linearly with the increase in drain-to-source voltage, obeying ohm's law - Here N channel acts like a simple resistors hence this is a linear increase in drain current.



(a) JFET with $V_{GS}=0V$ and a variable V_{DS} (V_{DD}).



(b) Drain characteristic.

At point B in figure, the curve levels off and enters the active region or saturation region where I_D becomes essentially constant.

As V_{DS} increases from point B to point C. The reverse-bias voltage from gate to Drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D constant.

Pinch-off voltage :-

For $V_{GS}=0V$, the value of V_{DS} at which I_D becomes essentially constant (point B on the curve) is the pinch-off voltage V_p. For a given JEFT, V_p has a fixed value.

I_{DSS} : Maximum Drain Current / (Drain-to-Source current with gate shorted).

After the pinch-off voltage, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This constant value of drain current is I_{DSS} and is always specified on JFET datasheets.

I_{DSS}: is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} = 0\,V$.

Breakdown:

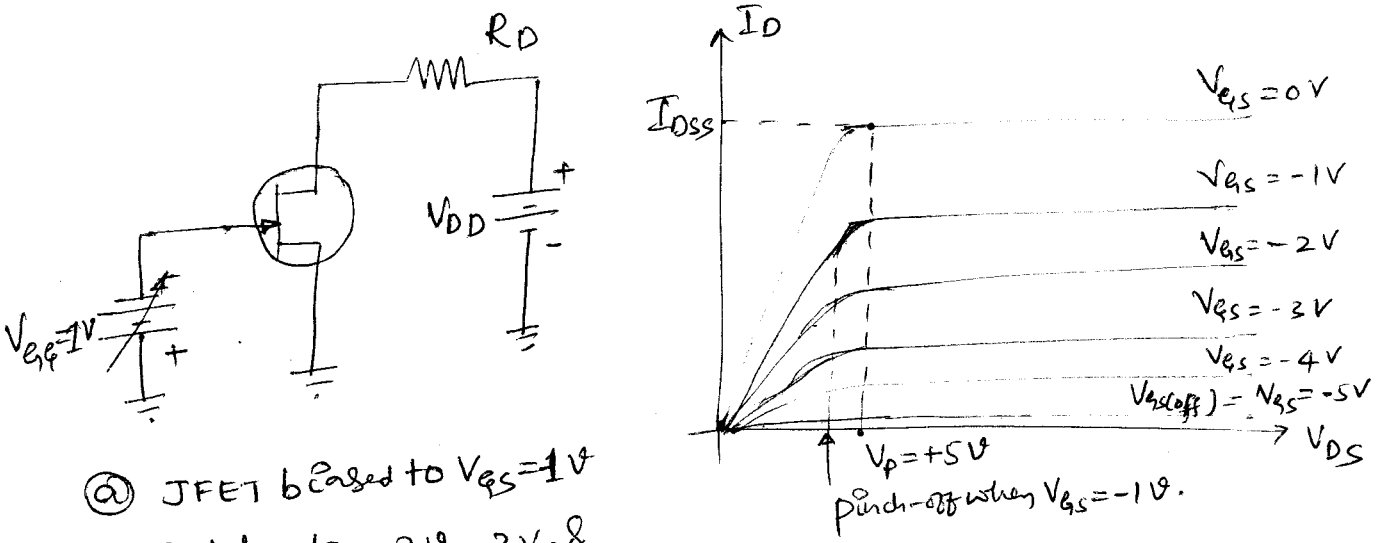
As shown in figure (b), breakdown occurs at point C when I_D begins to increase very rapidly with any further increase in V_{DS}.

Breakdown can result in irreversible damage to the device, so JFET are operated below breakdown & with in the active region (constant current) Between point B & C (in the graph). The breakdown point is shown with point C.

Now we connect a bias voltage, V_{GG} from gate to source as shown in figure (a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG} a family of drain characteristic curve is obtained. as shown in figure (b)

In figure I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel.

We observe that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_p. The term pinch-off is not same as pinch off -voltage V_p.., The amount of drain current is controlled by V_{GS}, as shown in figure.



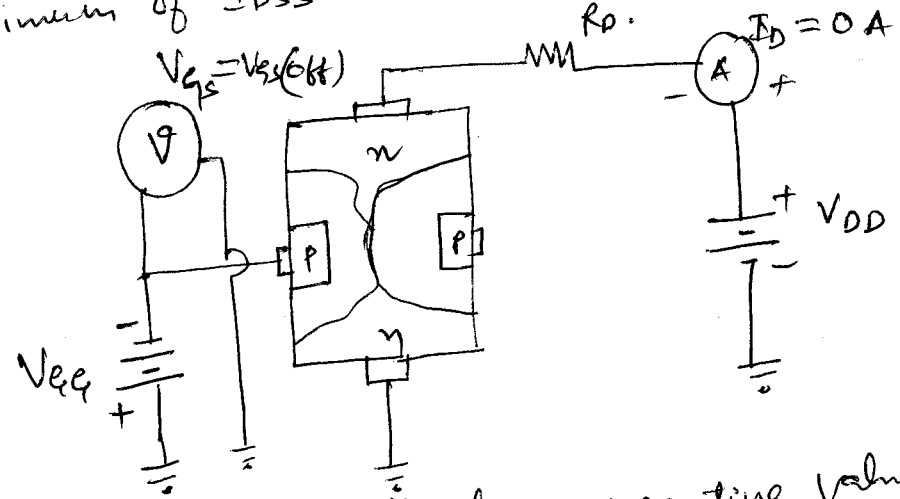
ⓐ JFET biased to V_{GS}=1V & later to -2V, -3V, & -4V and -5V.

ⓑ Family of drain characteristics curves.

Fig:- Drain characteristic curve with Applied V_{GS}.

Cutoff Voltage : $V_{GS(off)}$:-

The value of V_{GS} that makes I_D approximately zero is the cutoff voltage, $V_{GS(OFF)}$. as in figure ⓑ. the JFET must be operated between V_{GS}=0V and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.



when V_{GS} has a sufficiently large negative value. I_D is reduced to zero. this cut off effect is caused by widening of the depletion region to a point where it completely closes the channel. as shown in figure.

Note:-

Pinch-off voltage and cutoff voltage:-

The pinch-off voltage V_p is the value of V_{DS} at which the drain current becomes constant and equal to I_{DSS} and is always measured at $V_{GS} = 0V$.

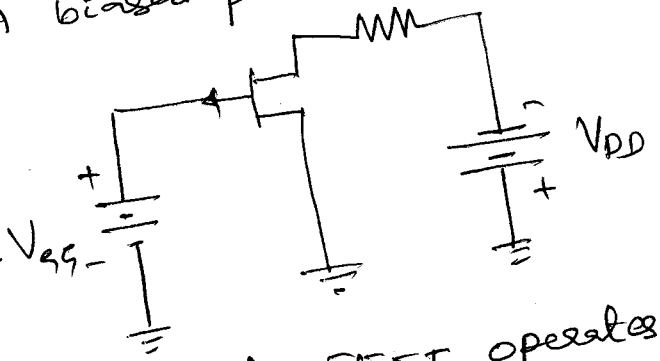
However the pinchoff occurs for V_{DS} values less than V_p when V_{GS} is non zero.

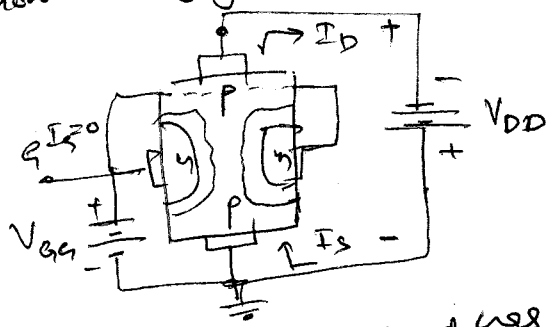
$V_{GS(off)}$ and V_p are always equal in magnitude but opposite in sign.

For Eg. if $V_{GS(off)} = -5V$. then $V_p = +5V$. as shown in figure.

Biasing of p-channel JFET:-

A biased p-channel JFET is shown in figure.





p channel JFET operates in the same way and has the similar characteristics as an N-channel JFET except that channel carriers are holes instead of electrons and the polarities of V_{GS} and V_{DD} are reversed as well as the direction of the output current I_D.

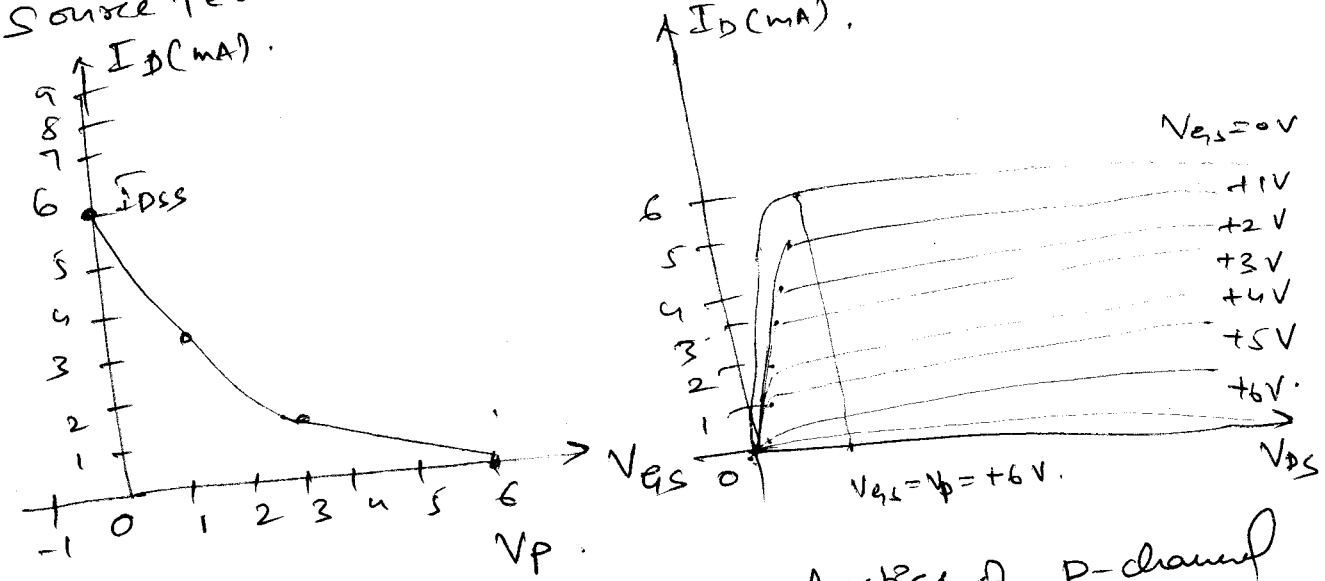
In p-type JFET holes acts as majority charge carriers, due to movement of these holes, current flow take place in transistor. p-channel JFET has three terminals with two n-type materials connected back to back as gate terminal & the p-type materials acts as source & drain ends.

As holes are majority charge carriers at $V_{GS}=0V$, the current flow is maximum when the positive V_{GS} is applied the current flow starts decreasing due to reverse bias at gate terminal and current flow is due to the negative V_{DS} across drain & source terminals.

Characteristics of p-channel JFET:-

From the drain characteristics it is clearly shown that at lower value of V_{GS} gain is maximum as the input voltage is (V_{GS}) increased gain automatically decreases as the channel gets shrinked.

At higher negative V_{DS} voltage the transistor starts to breakdown as the transistor fails to resist to the flow of current in the channel the breakdown is caused mainly because of higher positive voltage applied to source terminal.



Drain & Transfer characteristics of p-channel JFET.

Problem:-

(1) For the JFET in figure $V_{GS(off)} = -4V$ & $I_{DSS} = 12mA$ Determine the minimum value of V_{DD} required to put the device in the constant current region of operation when $V_{GS} = 0V$.

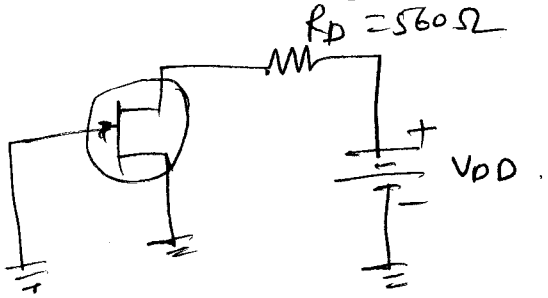


Figure:

Given:-

$V_{GS(off)} = -4V$

$I_{DSS} = 12mA$

$V_{DD} = ?$

$V_{GS} = 0V$.

Since $V_{GS(off)} = -4V$, then pinch-off voltage $V_p = +4V$.

The minimum value of V_{DS} for the JFET to be in its constant current region is

$$V_{DS} = V_p = 4V.$$

In constant current region with $V_{GS} = 0V$,

$$I_D = I_{DSS} = 12mA.$$

The drop across the drain resistor is

$$V_{RD} = I_D R_D = (12mA)(560\Omega) = 6.72V.$$

Apply Kirchhoff's law around the drain circuit.

$$V_{DD} = V_{DS} + V_{RD} = 4V + 6.72V$$
$$= 10.7V.$$

(2). In the above problem, if V_{DD} is increased to 15V. what is drain current?

Soln:- $V_{DD} = 15 = V_{DS} + V_{RD} = 4 + V_{RD}$.

$$V_{RD} = 15 - 4 = 11$$

$$I_D R_D = 11 \Rightarrow I_D = \frac{11}{560\Omega} = 0.0196A$$

or $\boxed{19.6mA. = I_D}$

JFET universal Transfer characteristics

Now, we know that a range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current. For an n-channel JFET, $V_{GS(off)}$ is negative, and for p-channel JFET, $V_{GS(off)}$ is positive.

The Transfer characteristics for a JFET can be determined experimentally, keeping drain-source voltage, V_{DS} Constant and determining drain current, I_D for various values of gate-Source voltage V_{GS}.

→ It shows relationship between V_{GS} and I_D.
→ This curve is also known as transConductance curve.

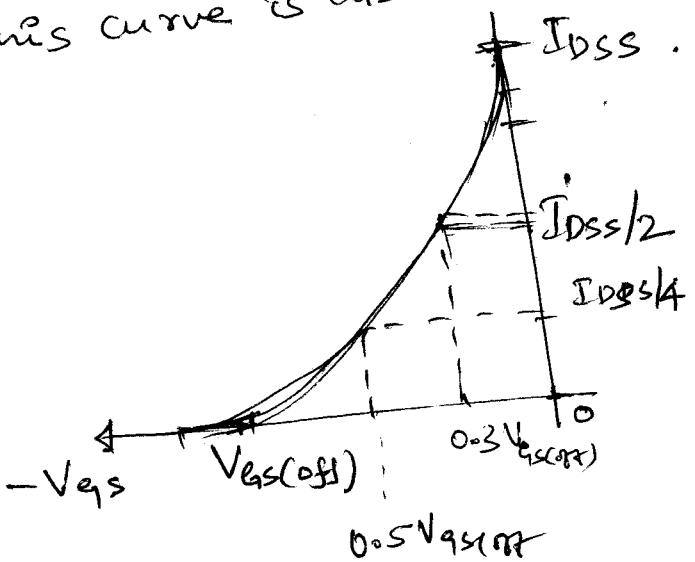


Fig → Transfer characteristic Curve (n-channel).

Observation :

→ Drain current decreases with the increase in negative gate-source bias.

→ Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$.

→ Drain current $I_D = 0$, when $V_{GS} = V_{GS(off)} = V_P$.

→ Drain current $I_D = I_{DSS}/4$ when $V_{GS} = 0.5\, V_{GS(off)}$

and $I_D = \frac{I_{DSS}}{2}$ when $V_{GS} = 0.3\, V_{GS(off)}$.

The Transfer characteristics curve can also be developed from drain characteristic curve.

This curve can be obtained by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch-off. as shown below in fig for a specific set of curves.

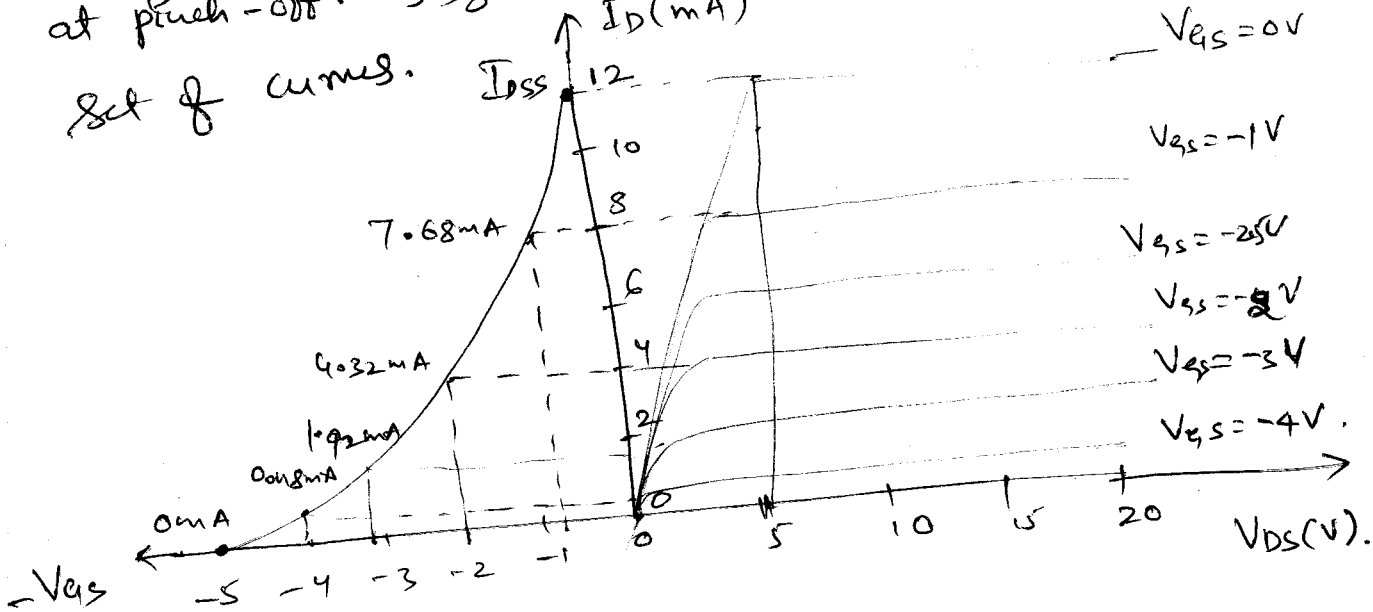


Fig:- Developing Transfer Characteristic curve from Drain characteristic.

The relationship between output drain current I_D and for any negative gate to source voltage V_{GS} in active region is given by Shockley equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Where,

V_{GS} = Applied gate-to source voltage.

I_{DSS} = Drain to source current for short circuit ($V_{GS}=0$) condition.

$V_{GS(off)}$ = Cut off voltage [-ve for n-channel].

V_{GS} = Gate-to source voltage.

Square Law Expression for I_D.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

observe the squared term in the equation, Because of its form, a parabolic relationship is known as a square law, and those JFET's and MOSFET's are called as square-law devices.

JFET Forward Transconductance

The Forward Transconductance (Transfer Conductance, g_m is the change in drain current (ΔI_D) for a given change in ~~drain current~~ Gate to source voltage (ΔV_{GS}) with drain-to-source voltage constant.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad \text{Siemens (S). or mho.}$$

$g_m = g_{fs} = Y_{fs}$ = forward transfer admitance.

important factor in determining the voltage gain of FET amplifier.

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

where

$$g_{mo} = \frac{2 I_{DSS}}{|V_{GS(off)}|}$$

Input resistance :-

JFET operates with its gate source junction reverse-biased, which makes the input resistance at gate very high. It is advantage for JFET.

$$R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right|$$

Where I_{GSS} → gate reverse current.

Input Capacitance Ciss

It is a result of the JFET operating with a reverse-biased pn junction.

A reverse biased pn junction acts as a capacitor whose capacitance depends on the amount of reverse voltage.

AC-Drain to Source Voltage

In Drain characteristics we know that, above pinch-off, the drain current is relatively constant over a range of drain-to-source voltages. Therefore, a large change in V_{DS} produces only a very small change in I_D. The ratio of these changes is the ac drain-to-source resistance of the device r_{ds}'.

$$r_{ds}' = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$r_{ds}' = \frac{1}{g_{os}} = \frac{1}{Y_{os}} =$$

This parameter also specified by the term output conductance or output admittance Y_{os}.

P1 For the typical JFET characteristics curve, Calculate the ac drain-to-source resistance for a JEFT biased at the origin if $V_{GS} = -2\,V$. given $I_{DSS} = 2.5$ mA and $V_{GS(off)} = -4\,V$.

Solution:

The transconductance for $V_{GS} = 0\,V$

$$g_{mo} = \frac{2 I_{DSS}}{|(V_{GS(off)})|} = \frac{2(2.5mA)}{|-4.0|} = 1.25\,mS$$

g_m at $V_{GS} = -2\,V$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

$$= 1.25mS\left[1 - \frac{-2\,V}{-4\,V}\right]$$

$$= 0.625\,mS$$

The ac drain-to-source resistance of the JFET is the reciprocal of the transconductance.

$$r_{ds}' = \frac{1}{g_m} = \frac{1}{0.625\,mS} = 1.6\,K\Omega.$$

P(2): For an N-channel JFET, $I_{DSS} = 8.7mA$, $V_P = 3\,V$ $V_{GS} = 1\,V$, Find the value of I_D.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8.7mA\left[1 - \frac{-1\,V}{-3\,V}\right]^2 = 3.87mA.$$

P③: For an JFET, $I_{DSS} = 9mA$ and $V_p = -8V$, using these values, determine the drain current for $V_{GS} = 0V, -1$ and $-4V$.

Given Data: $I_{DSS} = 9mA$, $V_p = -8V$.

$I_D = ?$ for $V_{GS} = 0V, -1$ & $-4V$.

Drain current is given by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

(i) For $V_{GS} = 0V$.

$$I_D = I_{DSS} = 9mA.$$

(ii) For $V_{GS} = -1V$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 = 9mA\left[1 - \frac{-1V}{-8V}\right]^2$$

$$= 9mA\left[1 - 0.125\right]^2$$

$$= 9mA\,(0.766) = \underline{6.89mA}.$$

(iii) For $V_{GS} = -4V$.

$$I_D = 9mA\left[1 - \frac{-4V}{-8V}\right]^2$$

$$= 9mA(1 - 0.5)^2 =$$

$$= 9mA * 0.25$$

$$I_D = 2.25mA.$$

P(4) For an 2N5459 JFET typical values of $I_{DSS} = 9mA$ and $V_{GS(off)} = -8V$ (maximum). Determine the drain current for $V_{GS} = 0$, & $-5V$.

Solution: given data; $I_{DSS} = 9mA$ $V_{GS(off)} = -8V$

Case ① For $V_{GS} = 0$.

$$I_D = I_{DSS} = 9mA.$$

Case ② For $V_{GS} = -5V$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 9mA\left(1 - \frac{-5V}{-8V}\right)^2$$

$$= 9mA\,(1 - 0.625)^2$$

$$= 9mA\,(0.375)^2$$

$$\boxed{I_D = 1.265625\,mA}$$

P(5). A JFET is operated at Q-point $I_{DQ} = 4mA$ & $V_{GSQ} = -3V$. Determine I_{DSS} if $V_P = -6V$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_{DSS} = \frac{I_D}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} = \frac{4mA}{\left(1 - \frac{-3}{-6}\right)^2} = \frac{4mA}{0.25}$$

$$\boxed{I_{DSS} = 16mA}$$

P⑥: For an N-channel JFET, $I_{DSS} = 8\,mA$; $V_P = -5V$

Determine (i) I_D at $V_{GS} = -2V$ and $-3V$

(ii) V_{GS} at $I_D = 3\,mA$ and $5\,mA$.

Solution:-

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

(i) I_D at $V_{GS} = -2V$

$$I_D = I_{DSS}\left(1 - \frac{-2}{-5}\right)^2$$

$$= 8mA\left(1 - 0.4\right)^2$$

$$= 8mA * 0.36$$

$$= 2.88mA.$$

$V_{GS} = -3V$

$$I_D = 8mA\left(1 - \frac{-3}{-5}\right)^2$$

$$= 8mA\left(1 - 0.6\right)^2$$

$$= 8mA * 0.16$$

$$= 1.28mA$$

$$\boxed{I_D = 1.28mA}$$

(ii). For $I_D = 3mA$

$$3 = 8\left(1 - \frac{V_{GS}}{(-5)}\right)^2$$

$$3 = 8\left(1 + 0.2V_{GS}\right)^2$$

$$1 + 0.2V_{GS} = \sqrt{\frac{3}{8}}$$

$$1 + 0.2V_{GS} = \pm 0.6123$$

$$V_{GS} = -1.94V \text{ \& } -8.06V$$

$-8.06V$ is neglected as it is greater than V_P.

$$\therefore V_{GS} = -1.94V.$$

For $I_D = 5mA$.

$$5 = 8\left(1 - \frac{V_{GS}}{(-5)}\right)^2$$

$$5 = 8\left(1 + 0.2V_{GS}\right)^2$$

$$1 + 0.2V_{GS} = \pm 0.7905$$

$$V_{GS} = -1.05V \text{ \& } -8.95V$$

$-8.95V$ is neglected as it is greater than V_P

$$\therefore V_{GS} = -1.05V$$

(7) In the JFET ckt shown, determine, the minimum value of V_{DD} required to put the device in the pinch off region. given that at $V_p = -4V$. $I_{DSS} = 12mA$.

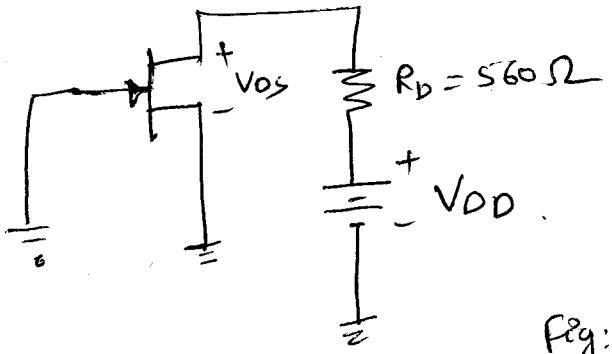


Fig:-

Solution:

In Fig.

We observed that $V_{GS} = 0V$

In pinch-off region with $V_{GS} = 0V$. we have.

$$I_D = I_{DSS} = 12mA.$$

The minimum value of V_{DS} for the JFET to be in its pinch-off region is $V_{DS} = V_p = 4V$.

Apply KVL to the output side

$$V_{DD} = I_D R_D + V_{DS}$$

$$= (12m)(560) + 4 = 10.72V.$$

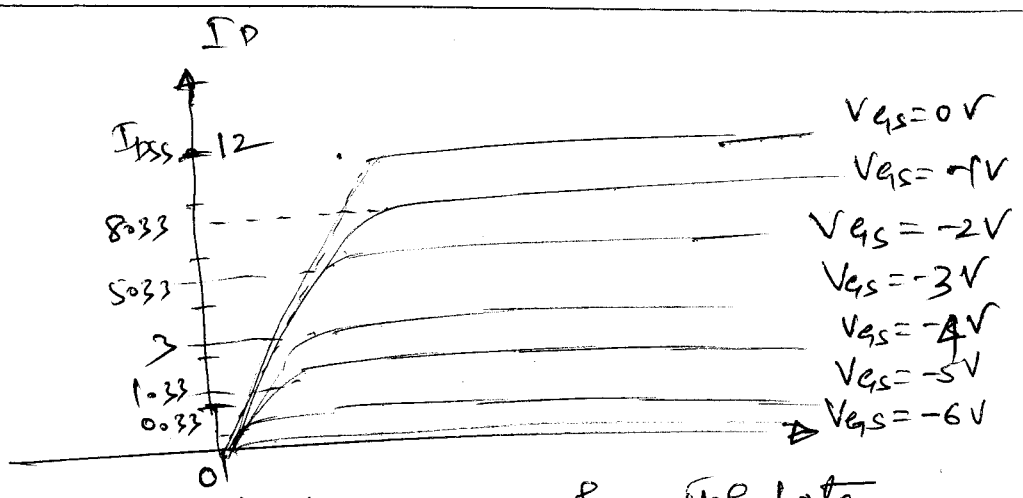
This is the minimum value of V_{DD} required to make $V_{DS} = V_p = 4V$, i.e to put the device in the pinch-off region.

(8): Find the transfer characteristics values of N-channel JFET. Given that $I_{DSS} = 12mA$ & $V_p = -6V$.

Soln:- we have $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

V_{GS} (V)	I_D (mA).
0	12
−1	8.33
−2	5.33
−3	3
−4	1.33
−5	0.33
−6	0

Then draw the graph.



Drain characteristic curve from the data calculated before.

(1) $V_{GS}=0V$. $\quad I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$

$= (12mA)\left(1-\frac{0}{-6}\right)^2$

$\boxed{I_D = 12mA}$

$V_{GS}=-1V$ $\quad I_D = (12mA)\left(1-\frac{-1}{-6}\right)^2$

$\boxed{I_D = 8.33mA}$

$-2V$ $\quad I_D = (12mA)\left(1-\frac{-2}{-6}\right)^2$

$\boxed{I_D = 5.33mA}$

$-3V$ $\quad I_D = (12mA)\left(1-\frac{-3}{-6}\right)^2$

$\boxed{I_D = 3mA}$

$-4V$. $\quad I_D = (12mA)\left(1-\frac{-4}{-6}\right)^2$

$\boxed{I_D = 1.33mA}$

$-5V$ $\quad I_D = (12mA)\left(1-\frac{-5}{-6}\right)^2$

$\boxed{I_D = 0.33mA}$

$-6V$ $\quad I_D = (12mA)\left(1-\frac{-6}{-6}\right)^2$

$\boxed{I_D = 0.mA}$.

MOSFET :

MOSFET stands for metal oxide semiconductor field effect transistor.

MOSFET has three terminal, Source, Gate & Drain.

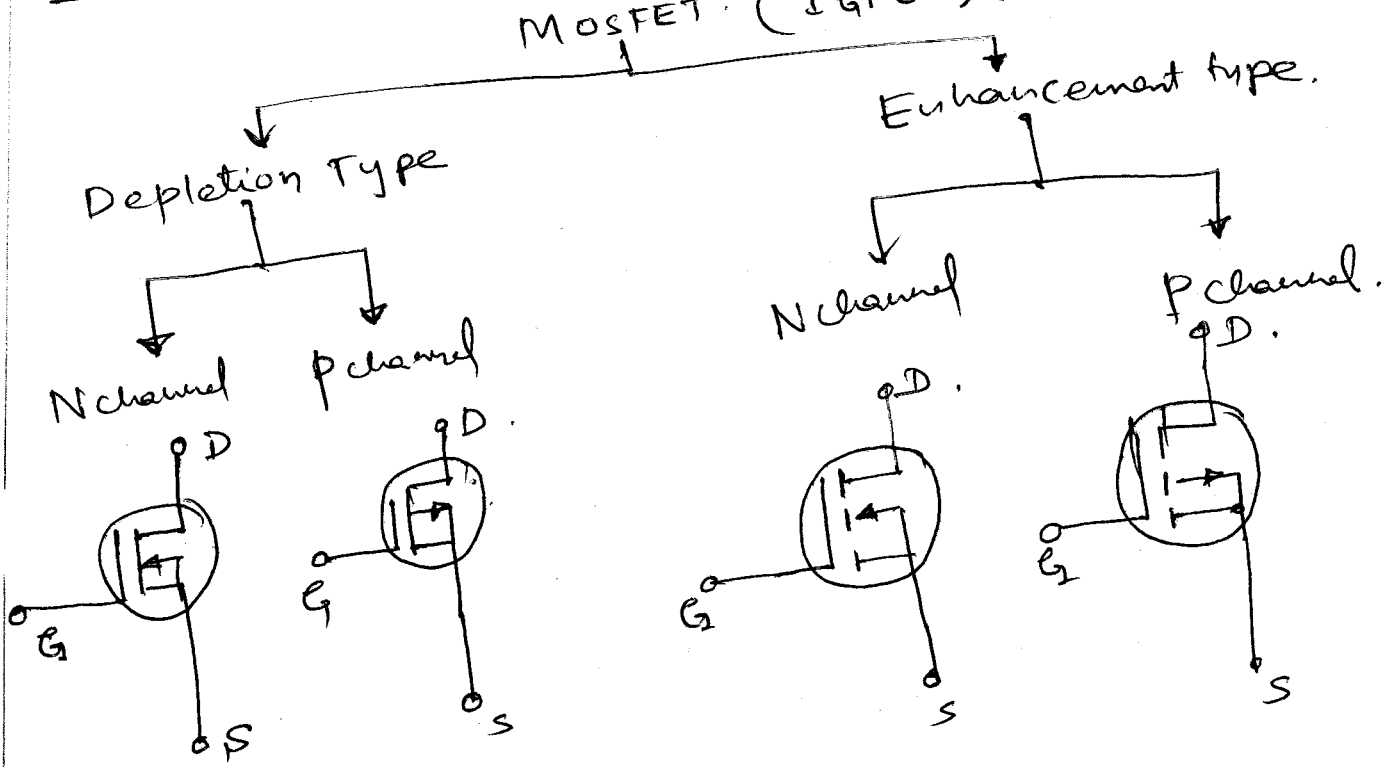
In MOSFET, the gate is insulated from the channel. But not in FET. Because of insulated gate, the gate current is even smaller than it is in a FET.

MOSFET is also called as insulated gate field effect transistor (IGFET). (or Insulated gate FETs).

MOSFET's are used in VLSI circuits such as microprocessors and semiconductor memories.

VLSI - Very large scale Integration.

Types of MOSFET



Basically two types

(1) Enhancement type MOSFET (normally-off).

(2) Depletion type MOSFET. (normally-ON).

Enhancement MOSFET

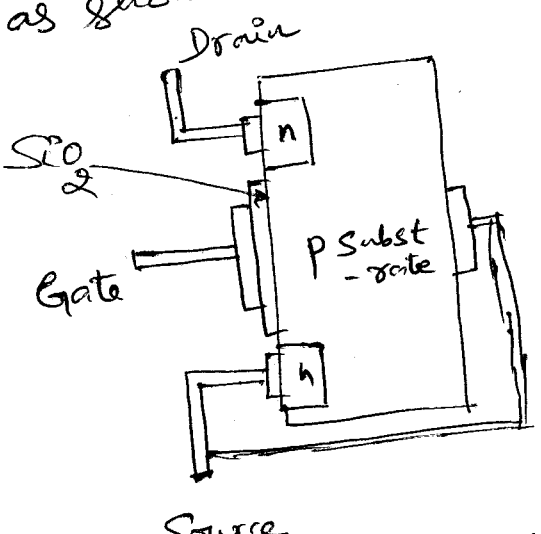
Construction:

The E-MOSFET operates only in the enhancement mode and has no depletion mode.

E-MOSFET has no structural channel.

Figure 1(a) shows the basic structure of the N-channel E-MOSFET.

In E-MOSFET, the substrate extends completely to the SiO_2 layer. For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer as shown in figure 1(b).



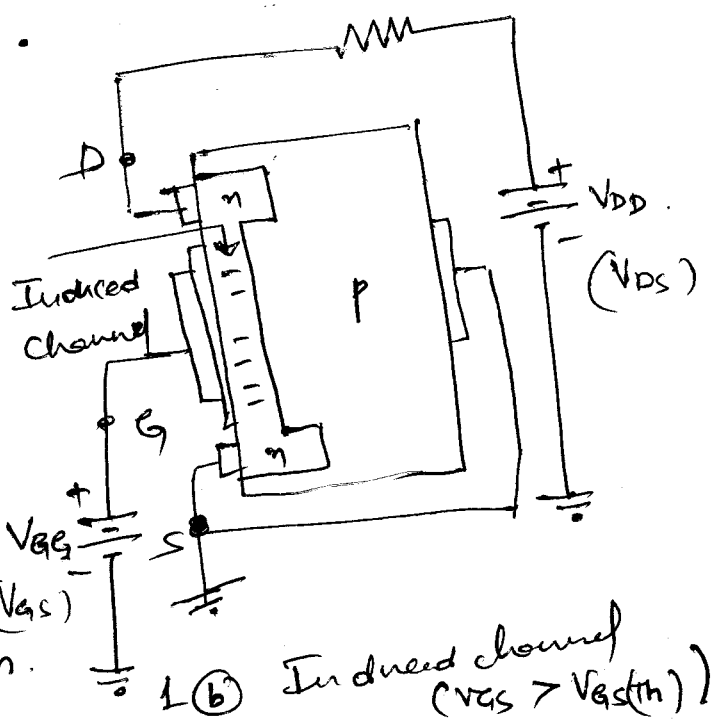


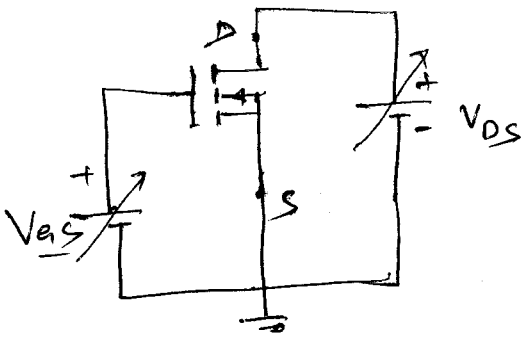
Fig. 1(a) Basic Construction. 1(b) Induced channel ($V_{GS} > V_{GS(th)}$)

The conductivity of the channel is enhanced by increasing the gate-to-source voltage, and thus pulling more electrons into the channel area.

Operation:-

Circuit Connection for E-MOSFET is shown in figure ③.

If some positive voltage is applied at the gate, it induces a negative charge in the p-type substrate adjacent to the silicon dioxide layer.



Fig③ Circuit connection

- The induced negative charge is produced by attracting the free electrons from the source.
- when the gate is positive enough, it can attract a number of free electrons and forms a thin layer, which stretches from source to drain.
- This layer of free electrons is called N-type inversion layer.
- The minimum gate-to-source voltage (V_{GS}) produces inversion layer is called as threshold voltage $V_{GS(TH)}$
- When $V_{GS} < V_{GS(TH)}$. $I_D = 0A$.
- when $V_{GS} > V_{GS(TH)}$. Inversion layer connects Drain & source we get I_D.

$$I_D = K\left(V_{GS} - V_{GS(TH)}\right)^2.$$

The relation ship between V_{DS} and V_{GS} is given by

$$V_{DS} = V_{GS(ON)} - V_{GS(TH)}.$$

Figure ④ shows the transconductance characteristics It is a graph of Input gate-to-source voltage (V_{GS}) and output drain current I_D.

For any gate voltage below the threshold value, there is no channel.

- E-MOSFET are called as "Normal-OFF state devices.
- The channel between Drain & Source is absent.
- The minimum voltage required to turn-ON MOSFET is called as "Threshold Voltage" $V_{GS(TH)}$.

The schematic symbol of n-channel & p-channel E-MOSFET's are shown in figure ②. The broken lines symbolize the absence of physical channel.

- An inward-pointing substrate arrow is for n-channel, & an outward pointing arrow for p channel.

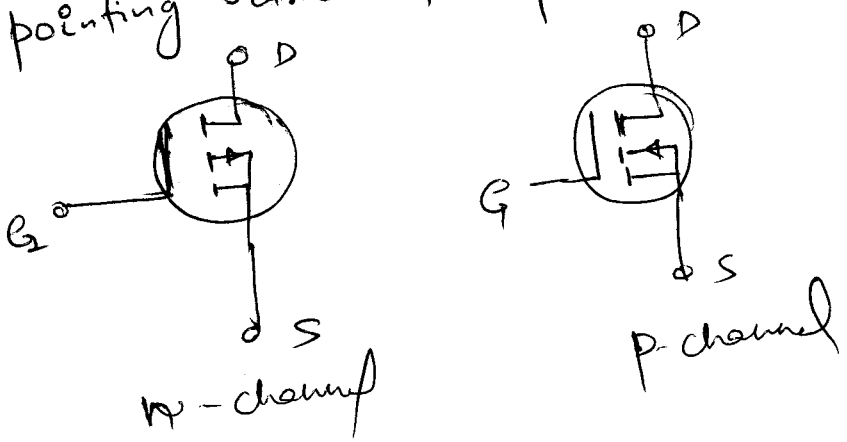


Fig ②. Symbol of E-MOSFET.

Here substrate is always shorted to source.

- For $V_{GS} > V_{GS(TH)}$, the drain current is given by the modified shockley equation.

$$I_D = K\left(V_{GS} - V_{TH}\right)^2$$

where $K = \text{Constant} = \dfrac{I_{D(ON)}}{\left(V_{GS(ON)} - V_{GS(TH)}\right)^2}$

V_{GS} = ON state gate-source voltage
$V_{GS(TH)}$ = Threshold Voltage of N-MOSFET.

- It is observed that, until $V_{GS} = V_{TH}$, there is no-drain current, EMOSFET operates in cut-off mode (open switch).

- When $V_{GS} > V_{TH}$, the channel is created and it becomes ON. This region of operation is called as Enhancement mode operation. i.e, as V_{GS} increases, output current I_D also increases depending upon the Drain current equation.

$$I_D = K \cdot (V_{GS} - V_{GS(TH)})^2.$$

Figure (5) shows the output characteristics of EMOSFET. It is a graph of output voltage (V_{DS}) and drain current (I_D) for a constant Gate-to Source voltage ($V_{GS} > V_{GS(TH)}$).

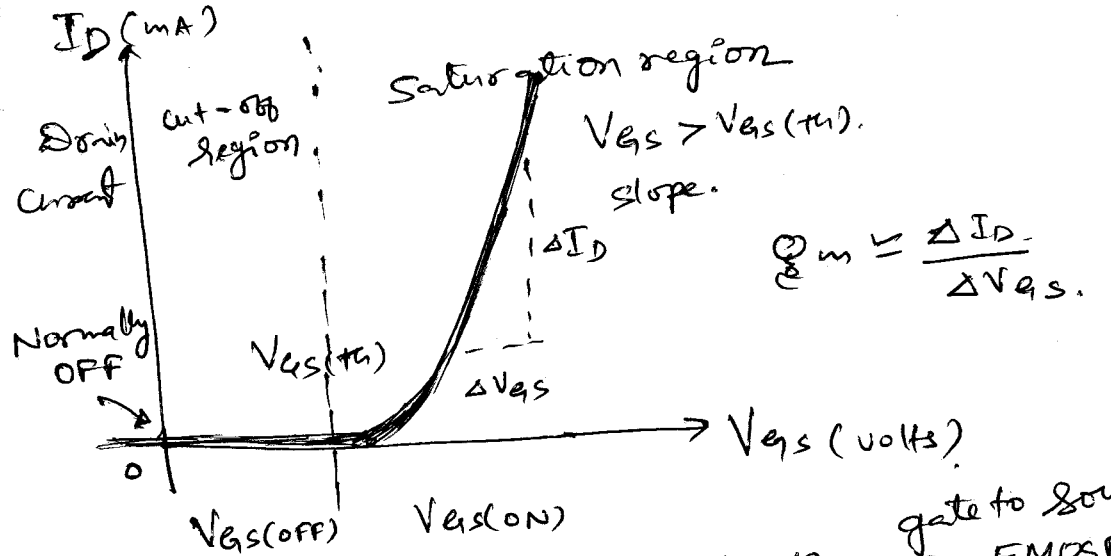


Fig (4). Transfer characteristics of gate to Source voltage of EMOSFET.

$V_{GS4} > V_{GS3} > V_{GS2} > V_{TH}$

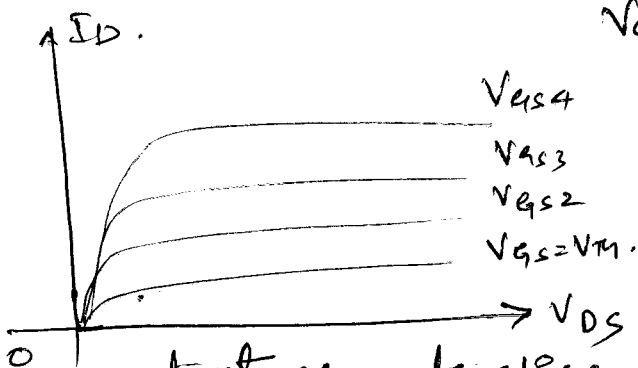


Fig (5): output characteristics.

p-channel EMOSFET

The construction of a p-channel EMOSFET is the reverse process of N-channel EMOSFET. i.e. here is now n-type substrate and p-doped regions under the drain and source connections.

- The terminals same as n-type EMOSFET. but all the voltage polarities & the current directions are reversed.

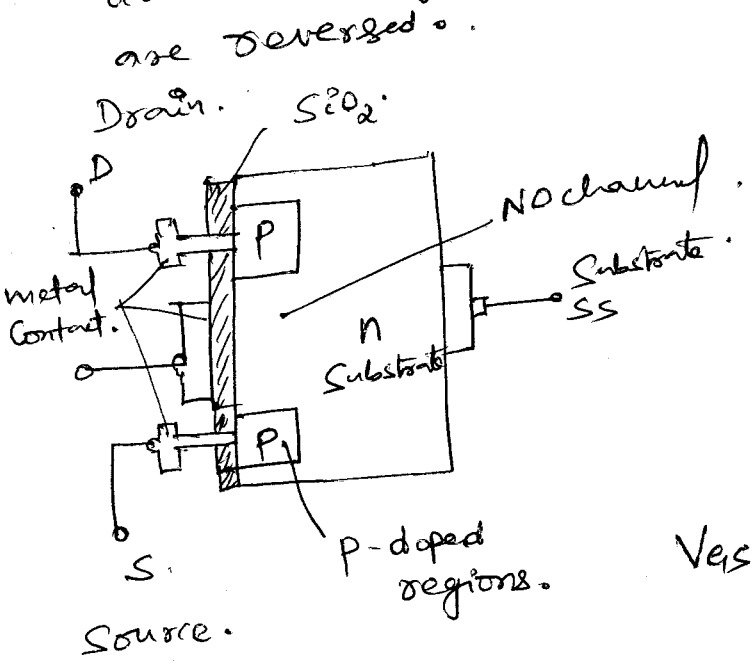


Fig 6(a) P-channel EMOSFET

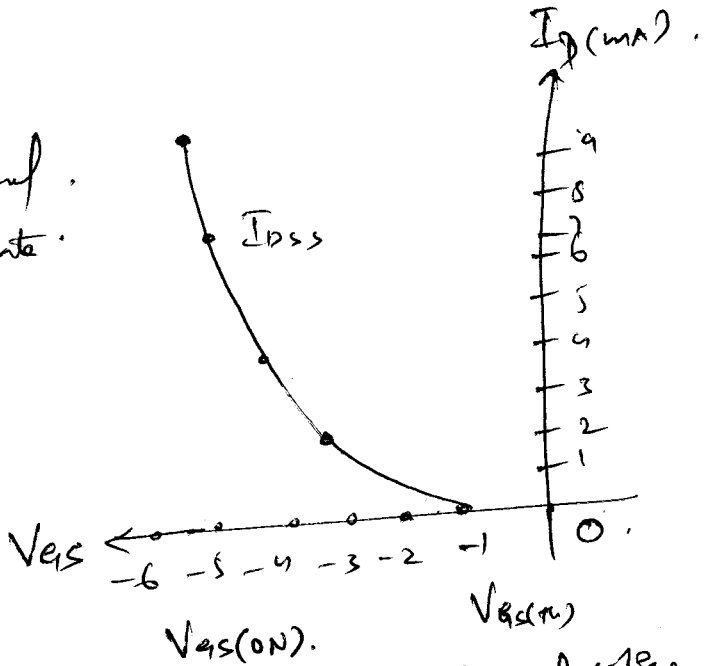


Fig (6b) Transfer characteristics

Construction of p-channel EMOSFET is shown in fig 6(a). Substrate and Source are shorted here. the Trans Conductance / Transfer characteristics are plotted in figure 6(b).

Depletion Type MOSFET : Constration.

- Another type of MOSFET is the depletion MOSFET.
- A physical channel is constructed between source & Drain.

Figure (7) shows the Basic structure of n-channel and p-channel DMOSFET.

→ The drain & source are diffused into the substrate material & then connected by a narrow channel adjacent to the insulated gate.

→ A DMOSFET N-channel device constration is explained below. A slab of p-type material is formed from a silicon base and referred to as the substrate.

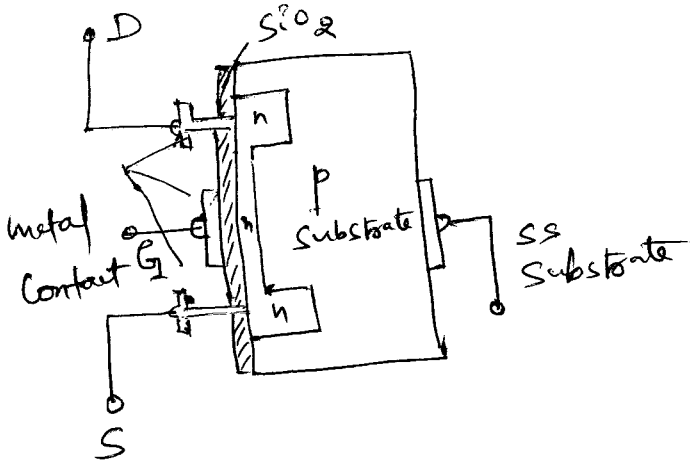
→ The source and Drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in figure (7) a

→ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin SiO_2 layer.

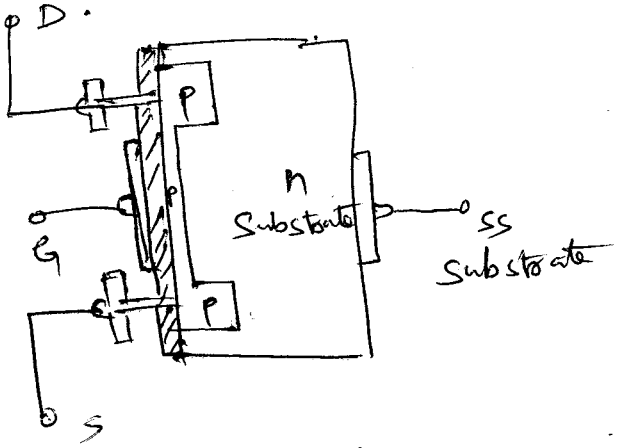
→ No electrical connection between the gate terminal and the channel of MOSFET.

→ SiO_2 layer in MOSFET accounts for very high desirable high input impedance of the device.

→ If entire structure acts as paralleled plate capacitors, then gate is one end and other by semiconductor channel. then plated is seperated by a dielectric (SiO_2) layer.



#(a) N-channel DMOSFET



#(b) p-channel DMOSFET

Operation :-

The DMOSFET can be operated in TWO modes.

(1) Depletion mode

(2) Enhancement mode.

It is also called as Depletion/Enhancement MOSFET.

- Since the gate is insulated from the channel, either a positive or negative gate voltage can be applied.
- When V_{GS} applied is negative N-channel MOSFET operates in depletion mode
- When V_{GS} applied is positive, then MOSFET operates in Enhancement mode.

→ They are generally operated in depletion mode

Depletion mode :-

The device operates in this mode, when gate voltage is zero or negative.

Fig 8 shows MOSFET with a negative gate to source voltage.

⇒ The negative voltage on gate, induces a positive charge in the channel.

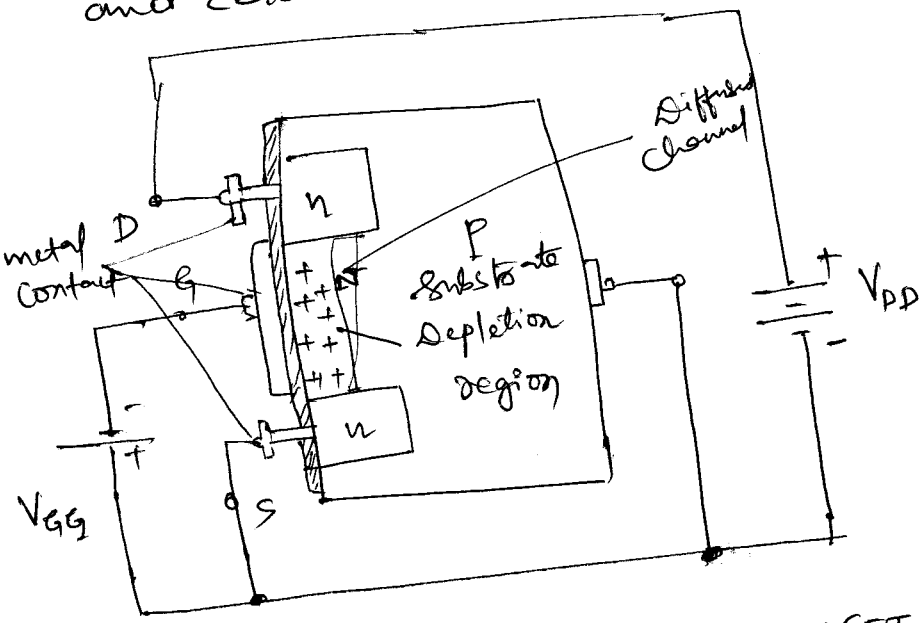
⇒ Because of this negative voltage, electrons in the vicinity of positive charge are repelled away in the channel.

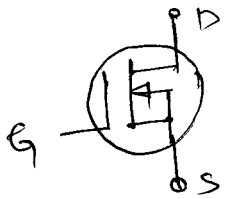
⇒ As a result of this, the channel is depleted of free electrons and Reduces the electrons resulting in the reduction of drain current I_D.

⇒ If $-V_{GS}$ increases means then I_D decreases.

⇒ At a sufficiently negative V_{GS} voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero.

⇒ Like n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero.





Depletion MOSFET Symbol

Figure ⑧ Depletion type MOSFET. with $V_{GS} \leq 0$. & applied voltage V_{DD}.

Figure 8 N channel MOSFET of depletion type. It offers very high input resistance. (about 10^{10} to 10^{15}). Significant current flows for given V_{DS} at V_{GS} of 0 volt.

when gate (i.e one plate of capacitor) is made positive, the channel (i.e the other plate of capacitor) will have positive charge induced in it.

Figure (9) shows the drain characteristic for the N-channel depletion type MOSFET in the common source configuration. These curves are plotted for both negative and positive values of gate to source voltage (V_{GS}). The curves for $V_{GS} \leq 0$, MOSFET operates in the depletion mode. If $V_{GS} > 0$, the MOSFET operates in Enhancement mode.

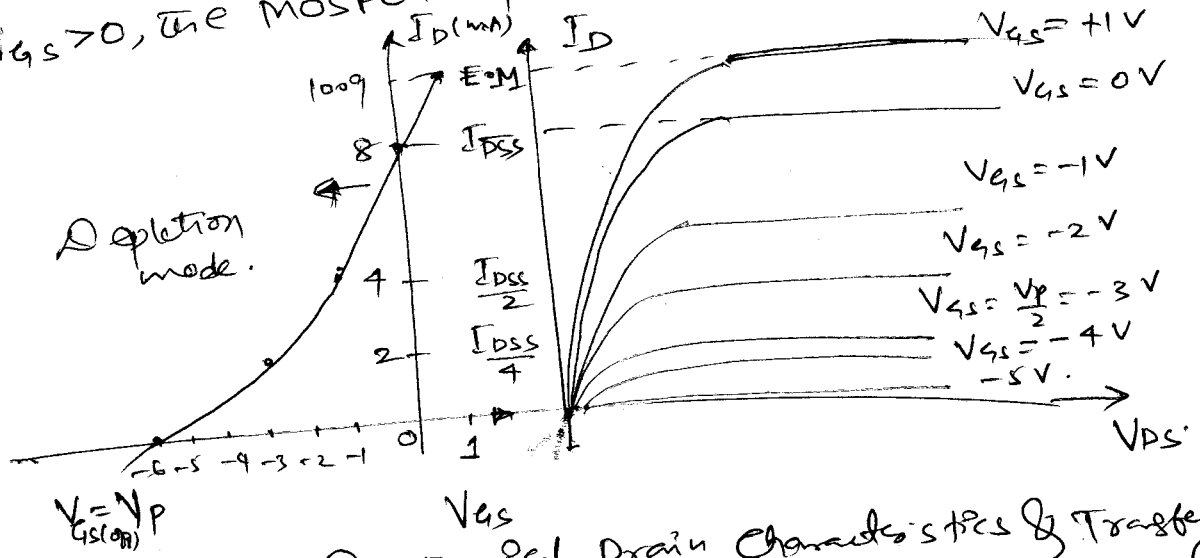
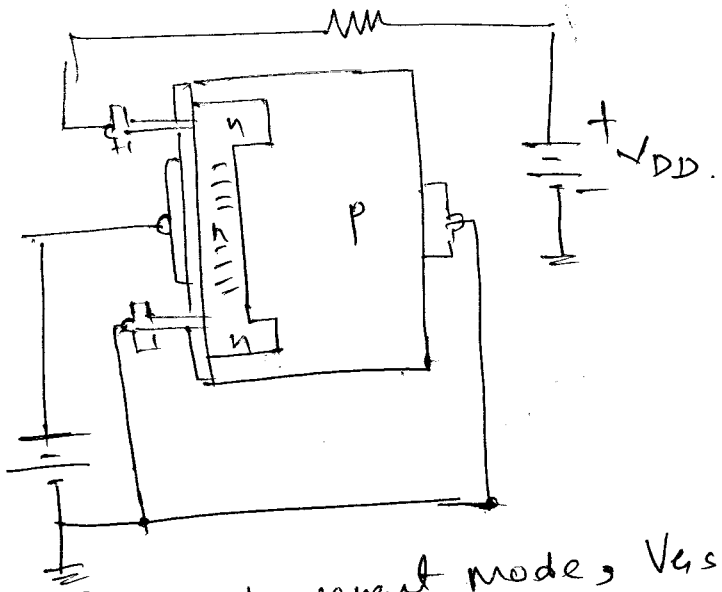


Figure (9). Typical Drain Characteristics & Transfer Characteristics for an n-channel depletion-type MOSFET.

Note:
EM-Enhancement mode

Enhancement mode:-

- MOSFET operates in this mode, when the gate voltage is positive as shown in figure (10).
- The positive gate voltage increases the number of free electrons passing through the channel. The greater the gate voltage, greater is the number of free electrons passing through the channel.



- This increases, ie enhances the conduction in the channel. Because of this fact, positive gate operation is called Enhancement.

Fig (10). Enhancement mode, V_{GS} positive.

As V_{GS} is made greater than zero ($V_{GS} > 0$), the current increases from I_{DSS} & becomes more positive constituting the positive drain current I_D. as shown in figure (9).

The depletion-MOSFET can conduct even if the V_{GS} is zero. Because of this it is also called as Normally ON MOSFET.

The Drain current is given by.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

where.

I_{DSS} →

V_{GS} →

$V_{GS(TH)}$ →

P(1): Draw the transfer and drain characteristics for an n-channel depletion-type MOSFET for the ranges of values $V_{GS} = -6V$ to $+1V$ with $I_{DSS} = 8mA$

Soln:- For depletion mode of operation, the drain current =

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

when $V_{GS} = -6$, $I_D = 8m\left(1 - \frac{-6}{-6}\right)^2 \cdot 1 = 0$.

$V_{GS} = -5$, $I_D = 8\times10^{-3}\left(1 - \frac{-5}{-6}\right)^2 = 0.2mA$

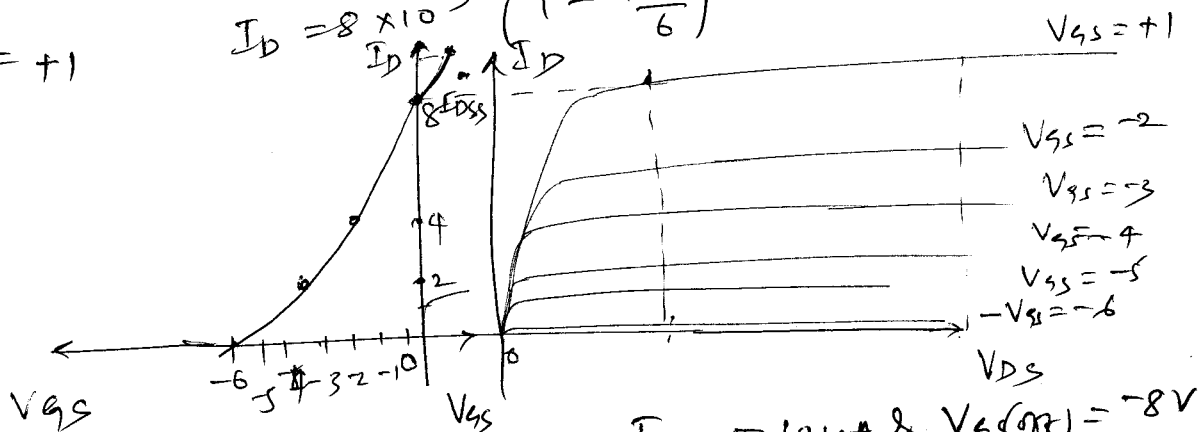
$V_{GS} = -4$, $I_D = 8\times10^{-3}\left(1 - \frac{-4}{-6}\right)^2 = 0.88mA$.

$V_{GS} = -3$ $I_D = 8\times10^{-3}\left(1 - \frac{-3}{-6}\right)^2 = 2mA$

$V_{GS} = -2$ $I_D = 8\times10^{-3}\left(1 - \frac{-2}{-6}\right)^2 = 3.55mA$

$V_{GS} = -1$ $I_D = 8\times10^{-3}\left(1 - \frac{-1}{-6}\right)^2 = 5.55mA$

$V_{GS} = +1$ $I_D = 8\times10^{-3}\left(1 - \frac{+1}{6}\right)^2 = 10.9mA$.



P(2). For an certain D-MOSFET, $I_{DSS} = 10mA$ & $V_{GS(off)} = -8V$

(a) Is it an n-channel or a p-channel

(b) Calculate the I_D at $V_{GS} = -3V$

(c) Calculate the I_D at $V_{GS} = -3V$.

Soln: (a) The device has a negative $V_{GS(off)}$, therefore, it is an n-channel MOSFET.

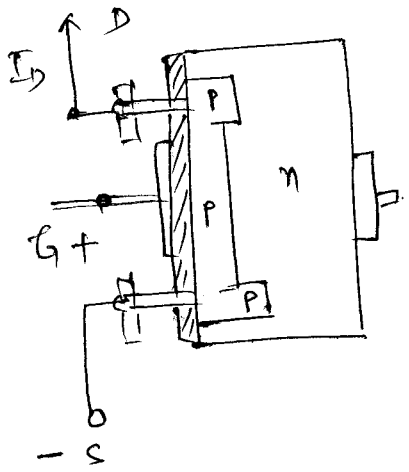
(b) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 10mA\left(1 - \frac{-3V}{-8V}\right)^2 = 3.91mA$

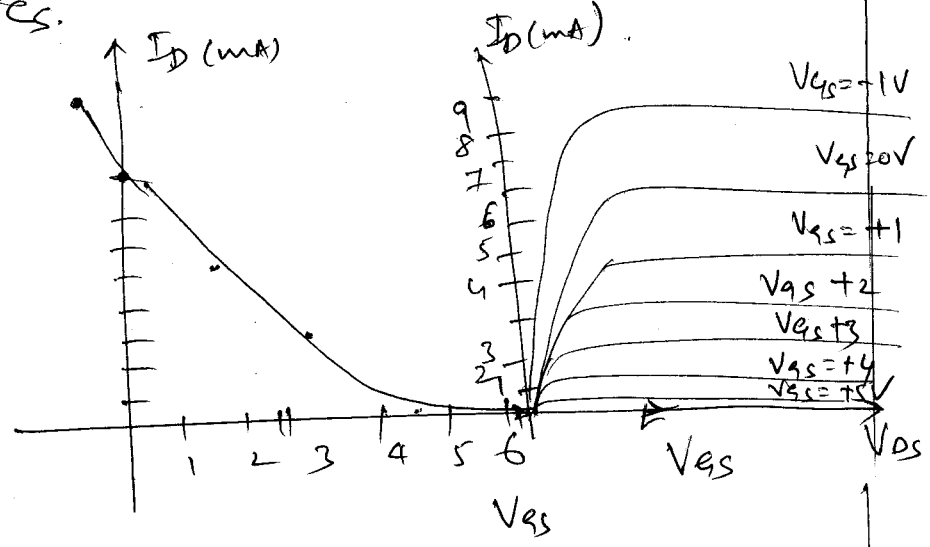
(c) $I_D = (10mA)\left(1 - \frac{+3}{-8}\right)^2 = 18.9mA$.

P-channel Depletion type MOSFET

The construction is exactly reverse of N-channel DMOSFET. Here n-type substrate and a p-type channel. The construction shown below.

P channel Depletion type MOSFET & typical Drain ~~and~~ transfer characteristics.





Comparision:-

Transfer characteristics

$V_{GS} = V_P = +6V$. Drain characteristics

Sl No.	FET	MOSFET	BJT.
1.	unipolar transistor	unipolar transistor	Bipolar transistor.
2.	High input impedance.	Comparatively higher than FET	Low input impedance.
3.	It is three terminal semiconductor device has Gate, source & Drain terminal	It has three terminal, Gate, source & Drain	It is also three terminal semiconductor device has, Base emitter & Collector.
4.	Gate must be reverse biased for proper operation	MOSFET may be Connected in Enhancement mode. that means that the device is not restricted to operating with its gate reverse biased.	Input Limit must be Connected in forward biased
5.	Voltage driven device	voltage driven device	Current driven device
6.	Noise level is small	Noise level is small	Comparatively more Noise than a FET.

CMOS Circuits

CMOS is a full form of complementary metal oxide semiconductor. CMOS is constructed using complementary & symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (CMOSFETs) for logic functions.

Here the two gates are connected to form the input terminal and two drains are connected to form the output terminal as shown in figure 1(a). The CMOS circuit offers two advantages:

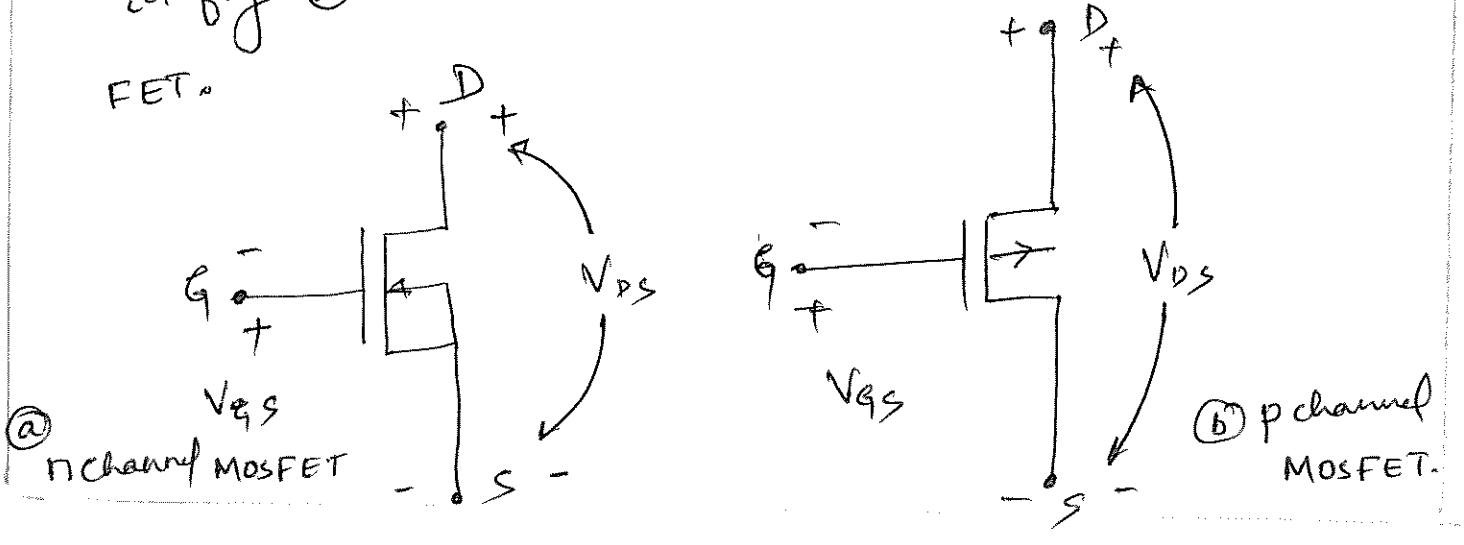
1. The drain current is very low and flows mainly during transistion from one state to the other (ON/OFF).

2. The power drawn in steady state is extremely small.

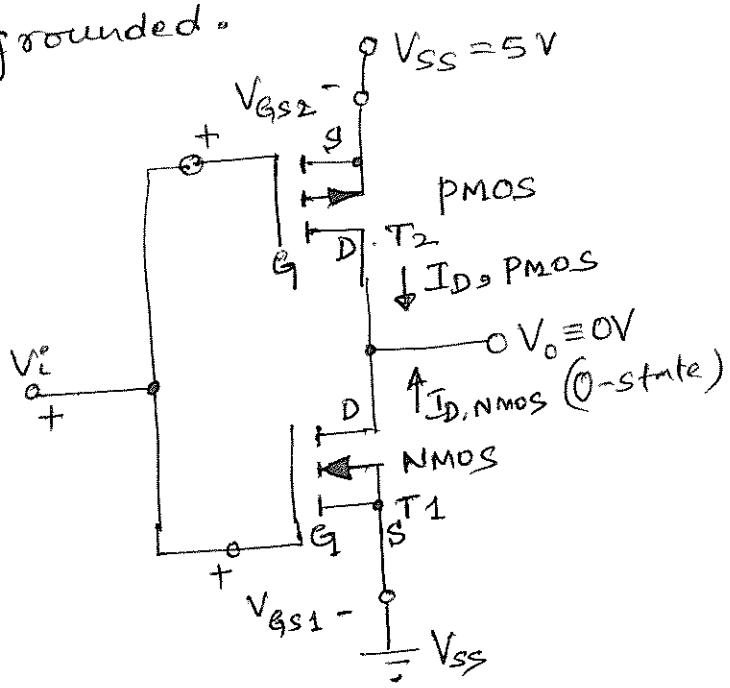
These two advantages, gained great popularity in digital circuits. Also used in Analog Circuit.

CMOS Application in Digital circuit :-

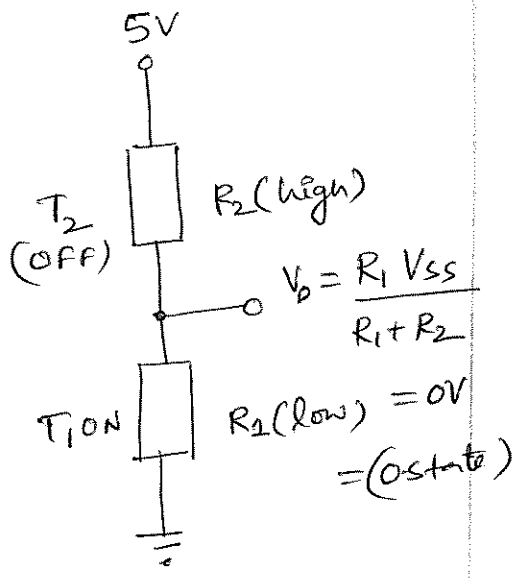
The one application is CMOS Inverter as shown in fig (2). The Digital Inverter used by nMOS & pMOS FET.



The source terminal of PMOS (T_2) is connected to $V_{SS} = 5V$, while the source terminal of NMOS(T_1) is grounded.



(a) CMOS inverter



(b) Equivalent circuit for $V_i = 5V$, state 1.

Fig: CMOS digital inverter

operation

when $V_i = 5V \Rightarrow$ 1 state

$V_{GS2} = 5 - 5 = 0V$ In this case T_2(pmos) is non conducting, OFF (ie V_T is negative, draws only leakage current, offers high resistance (R_2)

$V_{GS1} = 5V > V_T$.

T_1(nmos) is Conducting, ON, offers very low resistance (R_1). The equivalent circuit of CMOS digital inverter is shown in fig 2(b).

Output $V_o = 0$

$= 0$ - state.

From Fig 2 (b).

$$V_o = V_{ss} \cdot \frac{R_1}{R_1 + R_2}. \quad \text{because } R_1 = 0.$$

$$\simeq 0\ V.$$

For $V_i = 0$ Input $\Rightarrow$ state - 0.

$V_{GS2} = -5\ V$, T_2 Conducting (Low resistance)

$V_{GS1} = 0V$, T_1 nonconducting (High resistance)

output

$V_o = 5V \Rightarrow 1$-state.

We thus see that the ckt acts as an inverter, 1-state input produces 0-state output and 0-state produces 1-state output.

Here only one transistor is turned on in any of the output state. Here the transistors are connected in series, no current is drawn from the battery source in either of the two states.

only during state transition, the current is drawn from the battery. CMOS ckts draw extremely low power from the battery source and so their energy Consumption is very small. Hence the CMOS are used in digital application.

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Silicon Controlled Rectifier (SCR) -

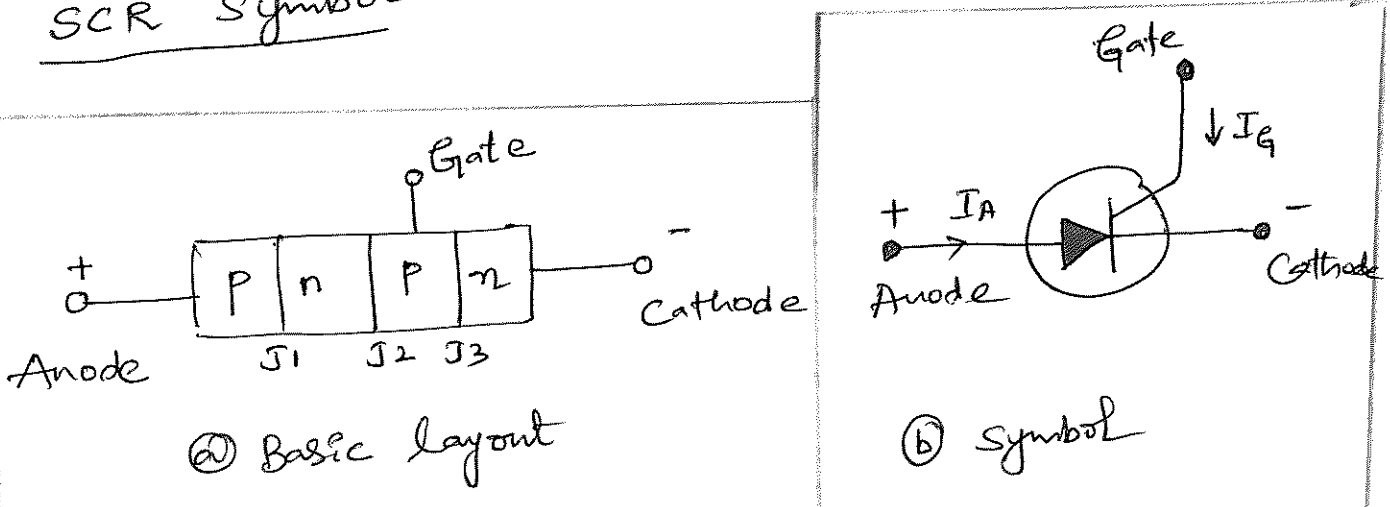
A silicon controlled Rectifier is a Four layer solid - state current controlling device.
It is also called as Semiconductor Controlled rectifier.

SCR along with associated circuitry has wide applications as.

>> Rectifiers
>> Regulated power supplies
>> dc to ac Conversion (inverters)
>> relay Control and
>> time delay circuits & many more.

SCRs are available to control power as high as 10MW with individual rating of 2KA and 1.8KV. The frequency range of 50KHz, are employed in high frequency applications like induction heating and ultrasonic cleaning.

SCR Symbol



(a) Basic layout (b) Symbol

Fig. 1 Silicon Controlled Rectifier (SCR)

Basic operation

The silicon is the material used for the fabrication of SCR, because of high temperate requirement of handling Large current and power. The Four layer arrangement of SCR is shown in figure 1(a) the "pnpn" structure is shown There are three p-N Junctions labeled J_1, J_2 and J_3 and three terminals namely Gate, Anode and Cathode.

The "anode" terminal of an SCR is Connected to the p-type material of PNPN structure, and the "Cathode" terminal is connected to the n-type layer, while "gate" of the SCR is Connected to the p-type material nearest to the Cathode. The Symbol of SCR is drawn in figure 1(b). The Symbol is similar to diode, the difference is indication of the gate terminal.

The Silicon Control Rectifier start Conduction when it is forward biased. The Forward Voltage is applied across the SCR. The Anode teominal is Connected to positive Supply & Cathode to negative teominal of the Supply. When positive clock pulse is applied at the gate terminal then the SCR turns ON

When SCR Forward biased by applying power supply The Junction J1 and J3 becomes foorward bias while the Junction J2 become reverse bias. when we apply a clock pulse at the gate teominal the Junction J2 becomes foorward bias and the SCR starts Condution.

The SCR turn ON and OFF very quickly. The foorward current Canode to Cathode) is offered a resistance as low as 0.01 to 0.1 Ω. The Dynamic reverse resistance of an SCR is as high as 100K Ω or more

Two transistor Model

Cross sectional view of an SCR with its four layers is shown in figure. 2(a). The middle n and p layers can be imagined to be subdivided into two halves, as shown by the dotted lines.

The SCR is now recognised as the device that Comprises one PNP and one NPN transistor. Here there is an electrical Continuity between the two halves of each of these layers, the base of PNP is Connected to the Collector of NPN; the Collector of PNP is Connected to the base of NPN while the gate is Connected to the base of NPN.

The equivalent two transistor circuit is shown in figure 2(b).

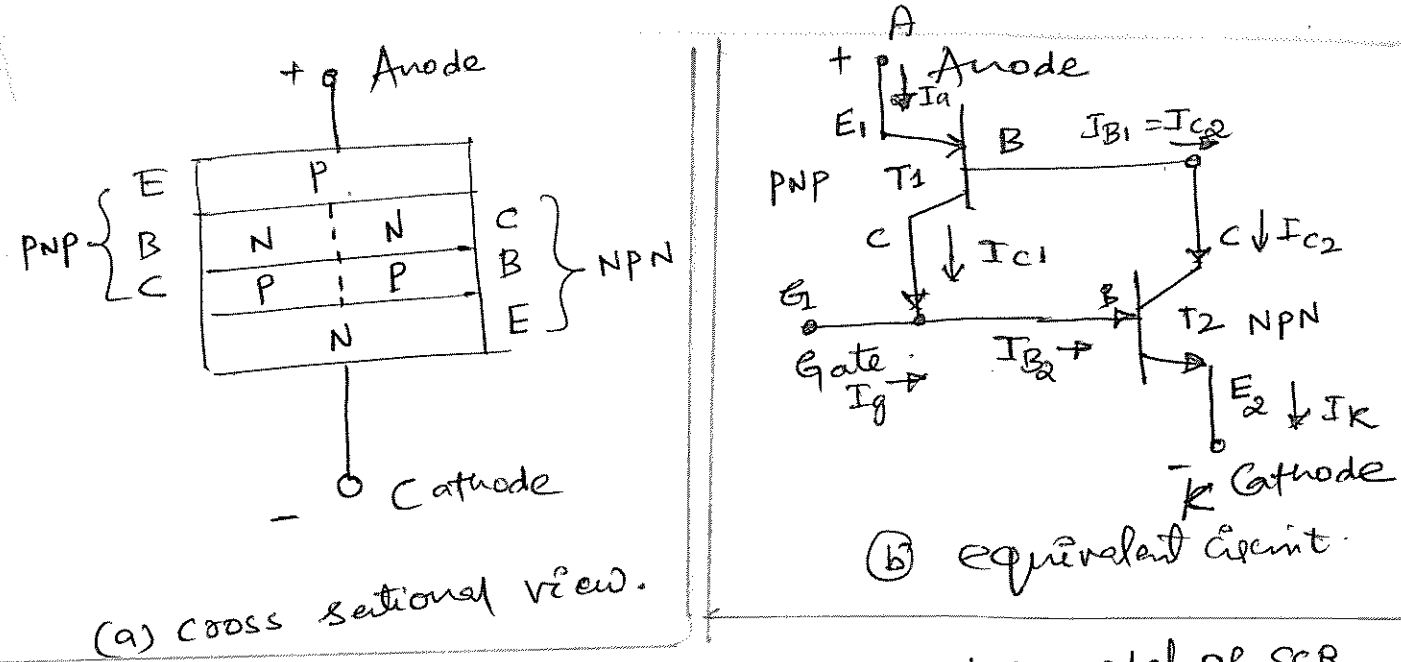


Figure (2). Two-transistor model of SCR.

Figure (2) is used to explain the action of the gate pulse I_G.

Switching Action;

Let a positive voltage V be applied to the anode (E1) and the cathode (E_2) and gate (G) be both grounded as shown in figure 3(a).

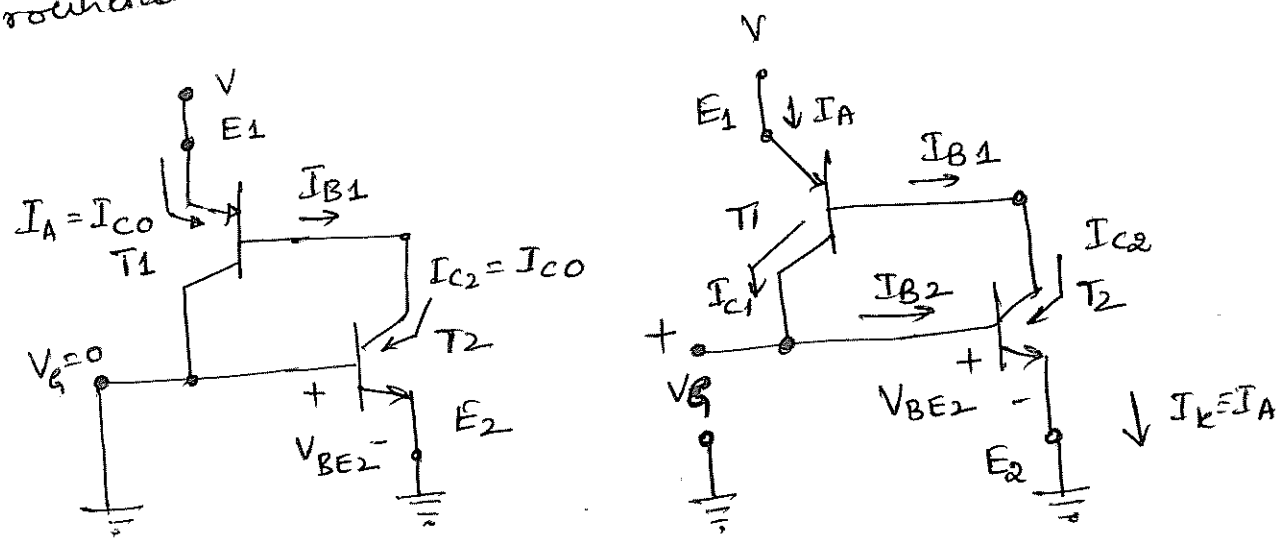


Fig (3) Switching action of a two-transistor SCR.

When $V_G = 0$, then $V_{BE_2} = 0$, The transistor T_2 is in OFF state. It means that CB junction of T_2, through EB Junction of T_1, is reverse biased.

Therefore, $I_{B1} = I_{CO}$ (minority carrier current) is too small to turn-on T_1. Thus both T_1 and T_2 are OFF and so anode current

$$I_A = I_{B1} = I_{CO}.$$

it is of negligible order. It means that SCR is in turn-OFF state, that is the switch between anode (E1) and Cathode (E2) is open.

Apply a voltage $+V_G$ at the gate terminal as shown in figure 3 (b).

As $V_{BE2} = V_G$, upon making V_G sufficiently large, I_{B_2} will cause T_2 to turn on and the Collector Current I_{C_2} becomes large.

As $I_{B1} = I_{C_2}$, T_2 turns on causing a large collector current I_{C1} ($I_A = I_{C1}$) to flow. This in turn, increases I_{B2} causing a regenerative action to set in (a positive internal feedback)

The result is that SCR is turned on, that is, the switch between the anode (E1) and Cathode (E_2) is closed (turn-ON).

The current I_A must be limited by the external circuit say a series resistance between the source & E1.

The turn-on time of an SCR is typically 0.1 to 1 μs.

However for high power devices in the range of 100 - 400A, turn on time may be 10-25 μs.

Turn OFF.

When the SCR is in Conduction mode, the gate is ineffective in turning it OFF.

The SCR turn-off mechanism is called Commutation and it can be achieved in two ways, namely

- Natural Commutation
- Forced Commutation.

The term Commutation means the transfer of current from one path to another. Commutation is the process of turning off a Conducting SCR.

Natural Commutation

Natural Commutation occurs in AC circuits. In AC supply, the current will flow through the zero crossing line while going from positive peak to negative peak. Thus a reverse voltage will appear across the device simultaneously which will turn off the thyristor immediately.

This process is called as Natural Commutation as SCR is turned off naturally without using any external components or circuit for commutation process.

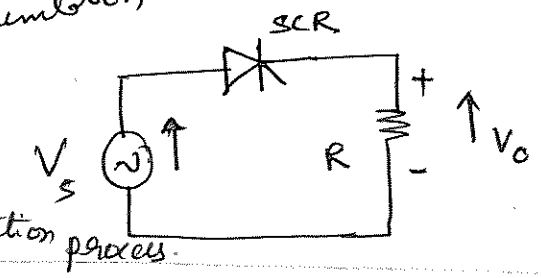


Fig: Natural Commutation process.

Forced Commutation

It is applied to DC circuits. Forced Commutation is achieved by reverse biasing SCR device or by reducing SCR Current below the holding current value.

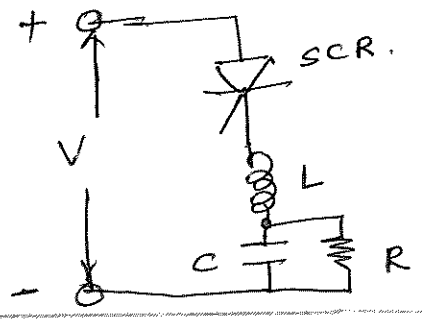
External circuit is used for forced Commutation process. It is called as Commutation circuit. The active or passive components / elements such as Inductance & Capacitance are used here. & these are called as Commutating elements.

Forced Commutation is applied to choppers & Inverters. Since SCR is turned off forcibly it is termed as a Forced Commutation process.

many different methods of forced Commutation are present namely

- self Commutation
- Impulse Commutation
- Resonant pulse Commutation
- Complementary Commutation
- External pulse Commutation
- Load side Commutation
- line side Commutation

An Example of self Commutation by resonating load is shown below.



Natural Commutation can be observed in AC voltage Controllers, phase Controlled rectifier and in cyclo Converters.

—o—

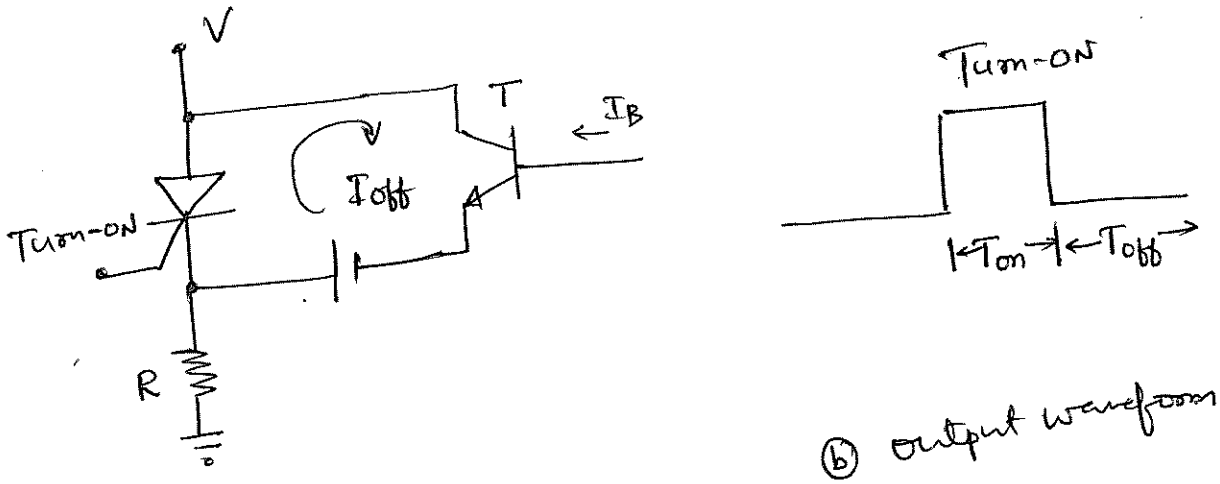
Another simple turn-off circuit is shown in figure below. Here a transistor and dc battery source in series are connected to the SCR.

When SCR is in condition mode (ON), $I_B = 0$ and when the transistor is off, it is almost an open circuit.

To turn off the SCR, a positive I_B pulse of magnitude large enough to drive the transistor into saturation is applied at the transistor base.

The transistor acts almost like a short circuit. This causes flow of very large I_{off} through the SCR in the opposite direction to its condition current. The total SCR current reduces to zero in a very short time causing it to turn off.

The Transistor has to withstand a large current but for a very short time. Turn-OFF time for an SCR is 5-30 μs.



(a) circuit. (b) output waveform.

Fig:- Turn-off circuit using SCR.

SCR characteristics and parameters

Forward & Reverse characteristics

Reverse characteristics

Consider a SCR shown in figure. Apply negative voltage to anode terminal and positive voltage to Cathode terminal.

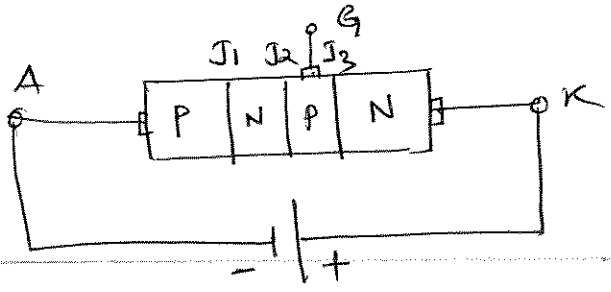
Then Junction J_2 is forward biased, while the Junction J_1 and J_3 are reverse biased.

When the reverse voltage $-V_{AK}$ is small, a small leakage current [of about 80 to 100 μA) flows, which is called as reverse blocking current.

If the reverse voltage is now increased, I_R (reverse Blocking current) practically remains Constant until $-V_{AK}$ becomes large enough to cause J_1 & J_3 to breakdown in the Zener or Avalanche mode.

As show in reverse characteristic curve, the reverse Current increases very rapidly when the reverse breakdown voltage is reached and if I_R is not limited, the SCR Could be damaged or destroyed

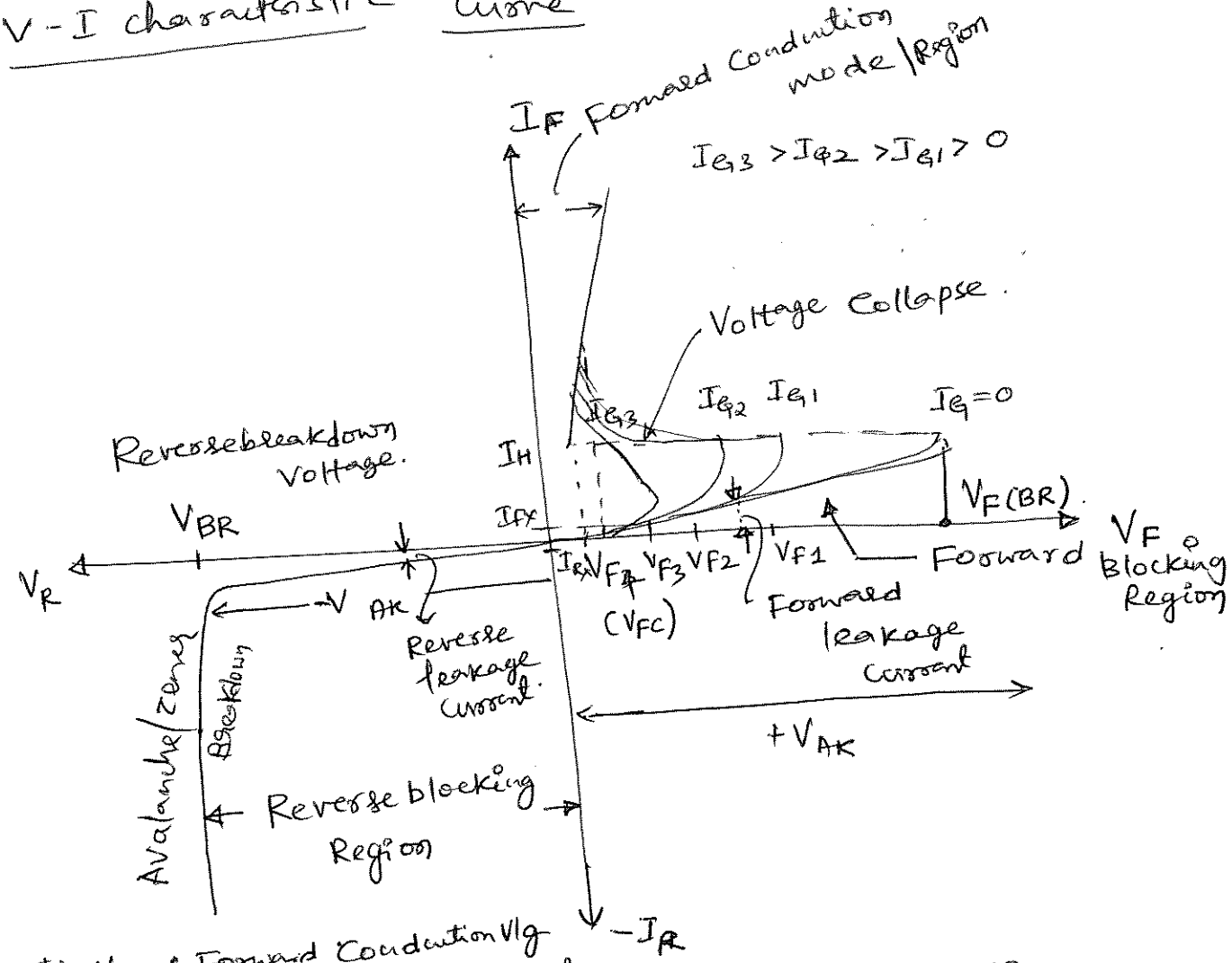
The Region of the reverse characteristics before reverse breakdown is Called reverse Blocking region.



J_1 & J_3 → Reverse Biased

J_2 → Forward Biased.

V-I characteristic Curve



Note:- V_{FC} : Forward Conduction Vlg
I_{RX} = Reverse Blocking Current

Figure : V-I characteristics.

If the SCR is forward biased with $I_G = 0$, the junctions J_1 & J_3 are forward biased and J_2 is reverse biased. If $+V_{AK}$ is very small, a small leakage current called as forward leakage current (I_{FX}) flows, which is almost equal to I_{RX} (reverse leakage current.

With $I_G = 0$, I_F remains at I_{FX} until $+V_{AK}$ is made large enough to cause the reverse biased Junction J_2 to break down. the Forward voltage at this point is called the Forward Breakover voltage $V_{F(BR)}$.

When $V_{F(BR)}$ is reached, the two transistors T_1 and T_2 are immediately switched on into saturation, and the anode cathode voltage falls to the Forward conduction voltage V_{F4} (V_{FC}).

The above method of triggering (Turn-ON) of transistor is called as Forward voltage triggering when in $I_G = 0$.

Consider when I_G is greater than zero. Then if $+V_{AK}$ is less than $V_{F(BR)}$, and $I_G = 0$ a small leakage current flows.

If I_G is made just slightly larger than the junction leakage currents, it will have a negligible effect on the level of $+V_{AK}$ for switch ON.

If I_G is made larger than the minimum base current required to switch the transistor T_2 ON, the SCR remains OFF until $+V_{AK}$ is large enough to forward bias the base-emitter junctions of T_1 and T_2.

As shown in figure. it is seen that when $I_G = I_{G3}$ $+V_{AK}$ must equal to V_{F3} for switch ON to occur.

The Forward conduction voltage, V_{F4} is made up ($V_{BE1} + V_{CE2}$) or ($V_{BE2} + V_{CE1}$).

The region of the V-I characteristics before switch-ON occurs is called the Forward Blocking region. & the region after switch-ON is called the Forward Conduction region. In FCR the SCR behaves as a Forward Biased Rectifier.

To switch the SCR OFF, the Forward current, I_F must be reduced below a level called Holding current I_H. The Holding current is the minimum level of I_F that will maintain the SCR in ON state.

(or)

Holding current is the value of current below which the SCR switches from the Conduction state to the forward blocking region.

As the gate current increases the triggering of the SCR will takes place for lesser value of the Anode-to Cathode voltage. as shown in figure.

$$I_{G3} > I_{G2} > I_{G1} > 0$$

and $$V_{F3} < V_{F2} < V_{F1} < V_{F(BR)}.$$

If a gate current greater than zero is maintained while the SCR is ON, lower values of holding current (I_{H1}, I_{H2} or I_{H3}) are possible.

Note:-

1. Forward Breakover voltage $V_{F(BR)}$ is the voltage at which for a given I_G, the SCR enters into Conduction mode. This voltage reduces as I_G increases. $V_{F(BR)}$ dependence on the circuit Connection between G and K terminals.

2. Holding current I_H is the value of current below which the SCR switches from Condution state to Forward Blocking regions of specified conditions.

3. Forward & Reverse blocking regions are those regions in which the SCR is open circuited and no current flows from anode to Cathode.

4. Reverse breakdown voltage corresponds to zener or avalanche region of a diode.

other parameters are
⟹ grid voltage, current and power are represented as

V_{GFM}, I_{GFM}, P_{GFM}.

Basically There are Different methods of Thyristor (SCR) turn-on techniques.

1. forward voltage triggering
2. gate triggering
3. dv/dt triggering
4. temperature triggering
5. Light triggering

Three modes are available

1. Forward Blocking mode
2. Forward Conduction mode
3. Reverse Blocking mode.

Application of SCR

These are used in rectifiers, regulated power supplies, dc to ac converter (inverters), delay Control & time delay Circuit.

The one application of SCR is variable Resistance phase control circuit is shown in below.

- Variable Resistance phase control,

upon triggering, an SCR (thyristor) permits flow of only forward current but blocks the current in reverse direction. The working of thyristor (SCR) this particular action is same as that of a diode.

On application of alternating voltage SCR causes rectified ac to flow but it needs to be triggered for each positive half cycle of ac.

It then produces constant dc (average value) current through load & dc voltage across load.

Adjusting the triggering time on positive half cycle of ac voltage would yield variable dc output.

This method is known as phase control.

A variable resistance phase control circuit is shown in figure. The SCR gate current is controlled through R and the variable Resistance R1.

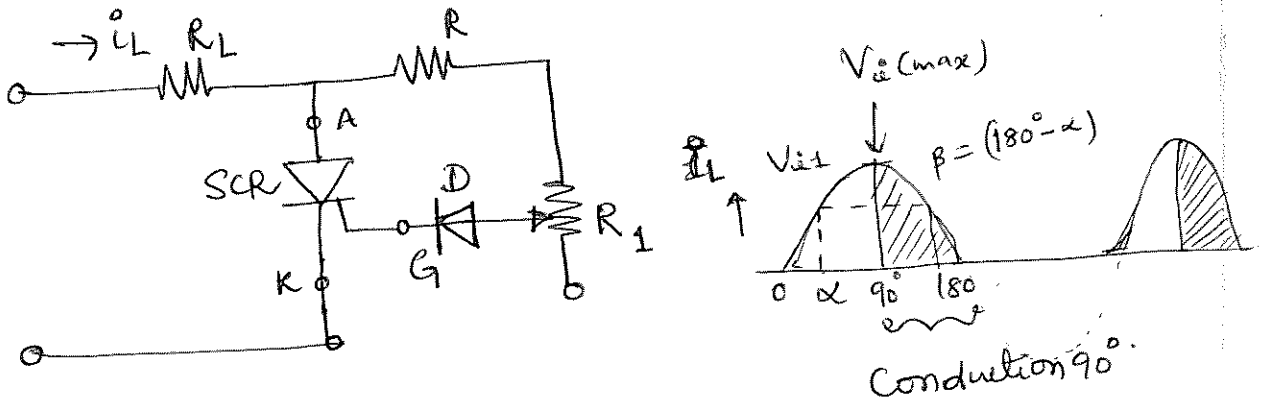
Let R_1 be adjusted to high value so that even at the peak value V_i (positive), $I_G < I_{G(TURN-ON)}$ and No Conduction take place.

Gradually Reduce R_1, then I_G increases to turn-ON SCR this triggering of SCR at a particular angle (time) of V_i take place.

Then SCR starts Conducting and Continues till V_i reaches zero (180°).

If we vary R_1, this allows the adjust of SCR firing angle from 0° to 90°. as shown in figure.

At R_1, corresponding to the firing angle of 90°, $V_i = V_i(max)$. If R_1 is adjusted for firing at α the firing will take place at angle $\alpha < 90^\circ$ but not at angle $\beta = (180^\circ - \alpha) > 90^\circ$ as the angle α is reached earlier in time on the V_i wave.
Hence this circuit is also known as half wave Variable resistance phase Control.



(a) Circuit (b) Firing angle

Figure : Variable resistance phase Control.

Thus $i_{L(dc)}$ Can be adjusted to the maximum value at 0° to the minimum value at 90°.
Diode is provided in the firing circuit to prevent the flow of reverse gate current.

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Commutation

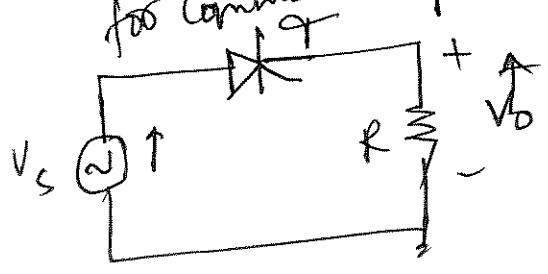
is the process of turning off a conducting SCR. There are two types of Commutation namely. current & voltage based.

Since the SCR is turned off forcibly it is termed as a forced Commutation process.

It occurs in AC circuits. ie when supply voltage is AC. Due to this SCR turns off when negative V/g appears across the SCR. Since there are no special CKTs needed to turn off the SCR, this type of Commutation is known as Natural Commutation

In AC supply, the current will flow through the zero crossing line while going from +ve peak to -ve peak. Thus a reverse V/g will appear across the device simultaneously which will turn off the thyristor immediately.

This process is called as NC as SCR is turned off naturally without using any external components or CKT or supply for Commutation process.



It is applied to DC CKTs. F.C is achieved by reverse biasing SCR device or by reducing SCR current below the holding current value. or by using active or passive components.

- Commutating elements such as inductance & Capacitance are used here.

FC is applied to choppers & inverters.

Following methods are used in F.C

- Self Commutation
- impulse
- Resonant pulse
- Complementary
- External pulse
- Load Side Commutation
- line Side Commutation.

NC can be observed in AC voltage Controllers, phase Controlled rectifiers & cycloconverters.

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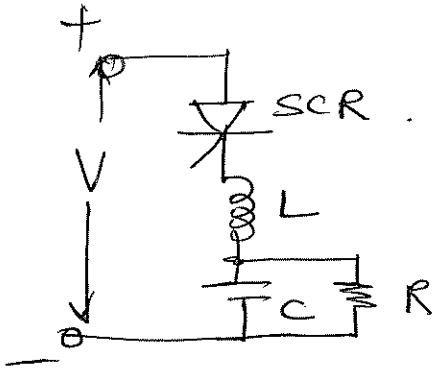

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External ckt is used for F.C process is called as Commutation process. is called as Commutation ckt & the elements in this ckt are called as Commutating elements