#### Module 3.

Operational Amplifiers & Applications

Introduction to Op-Amp

Op-Amp Input Modes

Op-amp parameters - CMRR

Input Offset Vottage and Current

Input Beas Current

Input Beas Current

Input and Ontput Impedance, Slew rate

(12.1, 12-2 of Text 2)

Application of op-amp.

Investing amplifies

Non-Envesting amplifies

Summer

Voltage follower Integrator Differentiator

Comparatos

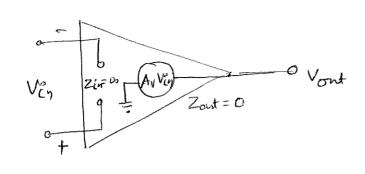
(6.2 of Text 1).

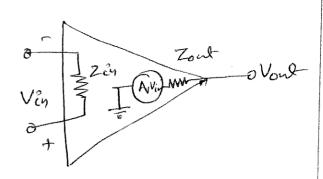
(RBT Levels: L1, L& & L3)

Operational Amplifiers

2

### Basic op-amp representation





(a) Ideal opamp representation. (6) partical - op-amp representation.

Op-amp Input modes.

Input signal modes These are determined by the differential amplifies input stage of the op-amp.

# (i) Differential mode:

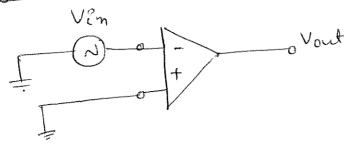
In the smode, either one signal es applied to an april With the other Enput grounded or two opposite polarity signals are applied to the inputs.

When an op-amp les operated En one single-ended différential mode, one Enput es grounded and a segnel voltage es applied to one other caput as shown En bigne.

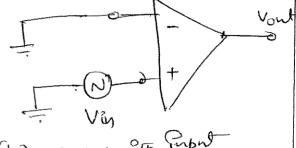
Case D: Here tre signal vottage Es applied to the Envesting Enpit, am Envented, amplified Segual voltage

Case Q: - Here one signal Es applied to the non-investing input when the Erveiling Enput grounded . a non Mrs. Asha K, Asst. Professor



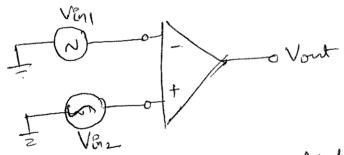


(a) SED M with input Councited to Enveeting terminal.



(b) SEDMWER Coput Connected to non-Enneting teeninal.

In the Double ended différential mode, two Opposite polarity (out of phose) signals are applied for Euports. as shown En figure. The amplified difference between the two Enputs appear on the output.



Double ended Differential mode

Common mode & - In Common mode, two Liquel Voltages of the same phases fleepremy and amplitude are applied to are two Enports, as shown in begins. when equal Enport seguels are applied to both Enports of they fend to Cancel, resulting En a zero output voltages

Y'MI=VI Vont = V, +V2 operation Vanz=12

Fig: Common Mrs. Asha K, Asst. Professor

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### Op-Amp palameler

In Common mode operation if some Enpud appears on the both the empit then only it produced by the op-amp Es zero. This is Colled Common-mode refertion. If any unidented signal appears commonly on both op-amp Enports, shen et réfects.

Common mode refertion means that this remounted Signal will not appear on one entput & distort the designed signal. Comman mode signals (noise) everture result of the pick-up of radiated energy on Enput lines, flow adjected lines, the GOHZ power lines, other Sources.

Common mode Réfertion Ratio [CMRR] Desired signal can appear on only one supert or with opposite polaritées on both Enpert leurs com be amplified 8 appear on output o but renwanted signed (noise) appearing wet the same polarity on both Enput & Concelled by

the op-amp & do not appeal on op-amp. The measures of an amplifier's ability to reject Common made rejection mode signals is Called as Common made rejection gation (CMRR].

CMRR. Siggests are measure of are op-amp's performance En referting unwanted common-modelsignals in the ratio of one open-loop differential voltage gain a Adams to one Common-mode gain Acm.

CMRR = Adm = '

CMRR & decibels (dB)

CMRR = 20 log ( Adm )

Différential mode gain le also called as open loop.
gain. (AOL).

open Loop Voltage gain: -

AOL 3 Of an op-amp Es the Enternal Vottege gain of the device.

It Es one votio of output voltage to Enput voltage when there use no external Components.

AOL = 200,000 (106dB). Also Called as large - Signed voltage gain.

CMRR of 100,000 for Example, means that the desired Exput signal (differential) is amplified 100,000 times more than the unwanted noise (common mode).

Problem 1. A costain op-amp has an open-loop differation Voltage gain of 100,000 & a common mode gain of Voltage gain of Express it in decibels.

SOL": ADL = 100,000 , Acm = 0.2

$$CMRR = \frac{AOL}{Acm} = \frac{100,000}{0.2} = \frac{500,000}{0.2}$$

Determine The CMRR and express of EndBforan op-amp were an open-loop differential vo Hage gain of 85,000 & a Common-mode gain of 0025.

AOL = 85,000, Acm=0-25. solution:

$$CMRR = \frac{AOL}{ACM} = \frac{85000}{0.25}$$

# Maximum Output voltage swêng (Vorp.p)]

wêter no Enput signal, The villant of an op-auro is Edealy OV. This is Called the quiescent output voltage when an Expert signal is applied, the ideal limits of tile peak-to-peak output signel are ± Vcc.

# Input offset vottage: - (Vos)

The Edeal op-amp produces Totalbets output for Zero Volts Enput. In a practical op-amp, however, a small de voltages Vout (error), appears at the output when no differential Emple voltage is applied. The main verson Es a slight mismatch of the baseemitter voltage of the differential amplifier input stage of an op-amp.

Vos -, Edeal Value Os/oIts

Vos > proutical value 2 m V vor less.

Expert offset voltage, vos : Es are differential de voltage required between one Enputs to force one output to Zero volts.

### Input Beas Current (IBEAS)

The Enput terminals of a bipolar differential amplifier are the transistor bases and, therefore, the input Currents are the base Currents.

The Enput beas current es the dc Current Required by the Enputs of the amplifier to properly operate the Herst Stage.

Input bêas current le me average of both Enput

currents . IBPas = Ib+ Ib2 V<sub>2</sub> of the state of the state

Ibins = 4+162

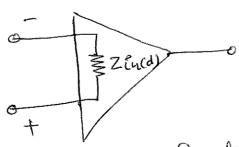
:- Input bias current is the average of the two op-amp Enput current.

Input Empedance :-

. differential Expet impedance . Common Eupet impedance.

Differential input impedance les one total resistance between the Envesting and the non-investing Enputs. as shown

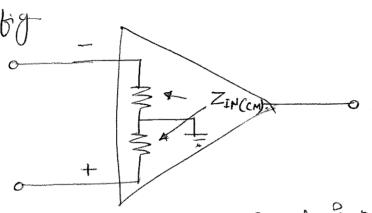
En fig.



Differential Enput Empedance

Differential Empedance Es measured by determining one change En blas current for a given change En differential Enput voltage.

The Common mode Enput Empedance is the resistance between each input and ground and is measured by determining one change in bias current for a given Change En Common-mode Expert Voltage. It ? shown in by



(b) Common-mode Enput Empedame.

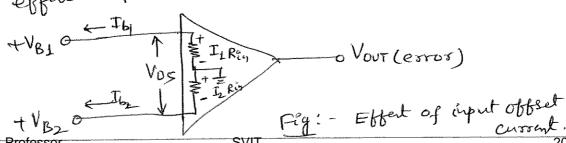
Input offset current: - Ios I deally, the two Enput beas currents are equal, and

Thus their différence les zero. practically op-amp, nowever, the beas currents are

. The Enput offset current, Ios, & the difference not exactly early. of the Enput beas Currents, expressed as an absolute Value.

Ios = | Ib - Ip) = | Ib1 - Ib2 |

The effect Enput Offset current is shown in figure



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The offset Voltage developed by the Enput offset current is

$$Vos = I_1 Rin - I_2 Rin$$

$$= (I_1 - I_2) Rin$$

$$Vos = Ios Rin$$

The error exected by Jos Es amplified by the gain Ar of the op-amp and appears En the output as

Vout (error) - Ay Ios Rin.

#### Output Impedance :-

The output Empedance Es the desistance viewed from the output terminal of the op-amp, as shown En bigure.

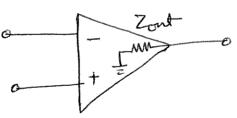


Fig. waters op-amp output Impedance

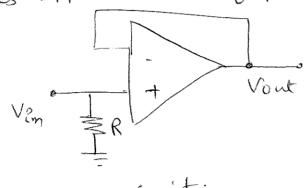
#### Slew vate:

The maximum vate of change of the output voltage En response to a step Eurpert voltage Es the stew rate of an op-amp.

- . The slew rate is dependent upon the high fleguing response of the amplifier stages with in the op-amp.
  - . Slew rate is measured with an up-amp Connected ay tiguse. ghown En

The openful here is the runty goin non investing Configuration

For step Enput, the slope on the output is Enneedly popostional to the upper critical frequent. sloppingesles as upper coictical feathermy decreases.



Vin o -- Vigge <- 4 >

@ Test cifcint.

Rig: - slow - sorte. meansened. @ step?uput Voltage & Osc resulting output voltage.

A pulse is applied to one Enput and the resulting ideal ontput voltage & Endicted En figure 6

The wider of the Expert pulse orust be sufficient to allow tre output to slew from êts lower limit to êts upper

At Es are time Enterval required for are output voltage to go from et lower leinet -Vmax to its upper limit + Vmax, once the Enput step is applied o

slew sate = <u>XVout</u> <u>St.</u>

These DVort = (+Vmax - (-Vmax))

runit = V/us.

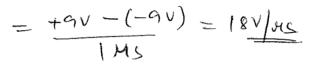
problem:

The output voltage of a colony op-amp appears 23 Shown in type En response to a step Enput adderwing 1 Vous (V) the slew rate.

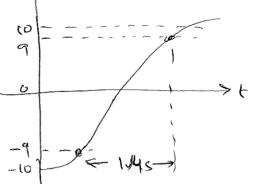
given Deute: at=145

Vman=9V -Vman=-9V

Slewrate = AVout



when a pulse Es applied to om opamp, are output Vo Haze goes from -8 V to +7 V & 0=7545. What is
The Slew rate?



Module -3: Introduction to operational amplifiers: 
The desired amplifiers: -

Ideal OPAMP, Inverting and non Enverting opamp aquits. opamp applications: Voltage follower, Addition, Subtraction, Integration, Differentiation, Numerical example as applicable

Key words: IC: Integrated Ciabuits
Introduction:

The op-amp is the Common name of operational amplifiers was designed in 1948 using Vacuum tubes. In those days, it was used in the analog Computers to perform a vasiety of mathematical operations such as addition, subtraction, multiplication etc. hence the name operational amplifier. Those op-ampase bulky, power Consuming and expansive.

The op-amp Es peanaps are most important & versatile Ic; it is used in amalog signal processing and amalog fittering.

The Ic version afopamp uses BJTs (Bipolaa Junction Transistors) and FETs which (Field effect Transistors) which are fabricated using semiconductor chip or water. The against design becomes very simple. These are low cost, small size, versatility, flexibility & dependability, op-amps are used in the fields of process control, communication, computers, power & signed sources, displays & measuring systems.

The op-amp & on excellent high gain D.C amplifier.

The Symbol of an op-amp & shown in figure (1).

It has two Enput teaminals, one is inverting teaminal (-)

Mrs. Asshork, Asst. Oprofessove sting (+), and one output teaminals. also

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requires The positive supply voltage terminal voc or +V. The negative supply voltage Learning -VEE OR

The op-amp can be defined as nigh gain, direct Coupled différence amplifier.

gain of op-amp = output voltage Enput voltage.

Dérent compled Endécates the op-amp can complify ségnals of zero frequeny means DC ségnals.

Difference amplifier means that the op-amp well have two Enputs and Freoutput. Es propositionar to the difference between the two Enput voltages.

1 + Vcc [ possessue supply voltage] Investing o OP-AMPS> Non-Enverting Enput. -VEE [negative supply voltages]

Fégure (1) op-amp symbol.

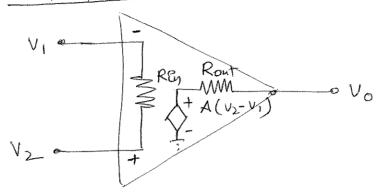
Commercially used power supply vottages are ±15V. Balanced dual supply. popular supply voltages are ±9V,

. The Enput at Enverting Input learning result in opposite polasify (antiphase) output. as shown in fig (2) Ven Antonior-amp

Invested ofp

while the Enput at non Enverting Input teemend result polasity (phase) output. as snown 3 fg 3.

The simplefied aquiet model of am op-amp is shown En figure (A). It has gain ob A, Euput resistance Rin and output resentance Rout Ana Edeal op-amp has A=00, REn=00 and Rato.



figner(4). ciquit model of op-amp - 1C 741 . The resistance Rin between the two onput levenings is Called Euput resistance of the op-amp. REn - En Ms range

. The Voltage source on the output side represents the output of the op-amp.

. The Voltage gain à Endécated along with the source Es Colled open 100p gain. A = Enorder 06106.

· term Vg-V2 & Called d'éfference Enput Voltage. The output propositional to difference between the two Enput

. The resestance En series with the voltage source Es The output resestance (Rout) of the op-amp. Rout es very low.

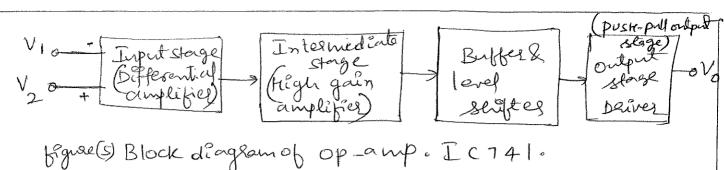
op-amp æchitature.

Commercial op-amps (IC) Consists of four cascaded block as shown En figure (5). It constists of · Input stage (Differential emplifies).

o Intermediate stage (High-gain amplifier)

Mrs. Asha K, Asst. Professor Daiver) & output salvigle.

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Input stage : -

· It requires high Enput Pupedence la avoid landing on the sources. It requêres two Enput terminals. It also Requeres low output impedance.

· All trese requirements are achieved by using the dual, Enput, balanced output Differential amplifier as Exput stage.

· function of a Differential amplifier is to amplify the different blatte two Expuls Equals. It provide Voltage gain of the amplifier. DA Consider of two BJT's with emitted terminal Connected together.

Intermedial stage 5-

. The output of the Enpirt stage daires the next stage which is an Entermediate stage. It is also on differential amplifier.

the overall gain lequilened of opening the very high. The Enput stage alone Cannot provide sneh a høyngaln. Intermediate stage provides om additionel voltage gary Regnissed. This stage consists of Caseaded amplifiers Called multistage amplifier used to get high gain.

Buffer & Level shifting stage

The land senter shifts are level of an eoutput of are Entermediate stage. This stage shifts the DC level.

. The land shifter stage brings the doc level down to ground potential, when nosegnal is applied to the Enpot terminals. Mrs. Asha, K. Asst. Professor. Chilter Skett Ny 164 Pa 1600 2018-19

output stage: -

The basec requilements are low output impedance, large a. c output voltage swing and high culent sourceing & sinking Capability.

push-pull Complements y amplifier ure also as Deriver slage The output stage provides une required power output. This Ps also colled power amplifier

#### IDEAL OPAMP.

Ine figure (6) shows ideal amplifier. It has two Enput Signalova & vz applied to Investing & ma Enverting teemines

V<sub>1</sub> → I<sub>1</sub>=0 Vd=0 OP-AMP Va o V + → Ig=0

I deal op-amp.

respectively. The Chalacteristics of Edeal op-amp age.

- @ Infinite Enput Empedanie (Rin= 00)
  - . The Enput Purpedance of The op-amp B Enforty.
  - . The Enput Purpedance & defined as the Purpedance Seen at the Enput teemends of the op-amp. The Empedance is a parameter outh opposes the flow of Current. Ren = 00, ensures that no aucht Complow Ento on Edeal op-amp.
- 6. Infinite voltage gain AOL=26. The differential open loop goin is infinite for Edeal op-amp. A = Vo. = D.

Mrs. AshafoAsstarojesson put vottage, the output vottage of op-amp becomes Enfinite.

E zero output Lapedance : [Ro=0] For Edeal op-amp Ro=0. This ensures that the output Voltage of the op-amp remains same, Exespertive ob the value of the load resistance Connected.

1 Infinite CMRR: - (P=0)

The latio of differential gain & Common mode gain is definied as CMRR.

if CMRR = 20, am Edeal op-amp ensures zero Common mode gain. Due to This Common mode nobse output voltage B zero for am Edeal op-amp.

€ zero roffset voltage (Vios = 0)

The presence of the small output Voltage though VI=Vz=0 Es Colled an offset Voltage. It is zero for an ideal op-amp. This ensures zero output for zaoluput signal Voltage.

- B. Temperature ûndependency: The characteristics of op-amp do not change wear temperature.
- 90 Infinite Bandwidter

The large of flequent once which the amplified performance it satisfactory & collect Bandwidth o Bandwidth = Co. This means that operating ferequent range & from otors.

This ensures that the gain of the op-amp will be constant over the frequent range from d.C (Zero frequent) to Enfinite frequent. So op-amp con amplified d.C as well as a.c. signals.

(B. Matched Transistors.

The transistors used in différence amplifier are identifée

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### (i). Infinite Slew rate: (S=00)

Slew late End Edes of the Rate at which the output Varies.

"Infinite slessate Endicates and the output Voltage Can change strumtomeonsly with the changes in The Enport Voltage. 11.

## (PSRR=0)

PSRR Es défined as the latio ob the change En Expert Obb Set voltage due to the change En Supply voltage producing it, keeping other power sopply voltage Constant. It is also Capled as power supply sensitively or Supply voltage Refertion ratio (SVRR). unit -mv/v or lev/v ideal value = 0.

I Deal characteristics for Support	Thas p syntol	O Ideal Values	2mV. praeticof	
Sl. NO chalanteristics ?  I open loop voltage gain	Aor	06	2×105	
1 Open 2000 2. Imput Empedance	Rin	Co	2MQ_	
output Impedance	Ro	0	7552	
Thouset Voltage	Vgos	0	2mV.	
Randwidth.	BW	Do	IMH3	
CMRR	S	<b>⊳</b>	90 dB.	
Slew Rale	S No DCPR	<u>∞</u>	304VIV.	
Ib o sont				
Typical passing of 44.				
Asha K, Asst. Professor SVIT	/(	20 de = 10	2018-19	

I Deal op-amp [Op-Amp Input Modes AND parameters] · Differential amplifier (DA). An amplifies which complifies The difference between the two Empit & Egnal. Hence o Et Es colled DEfferential (or Difference) amplified. apply two Exput signal to DA while No Es The single ended output : Each signed is measured with respect to ground. Vod (Vg-VA)

Vod (Vg-VA)

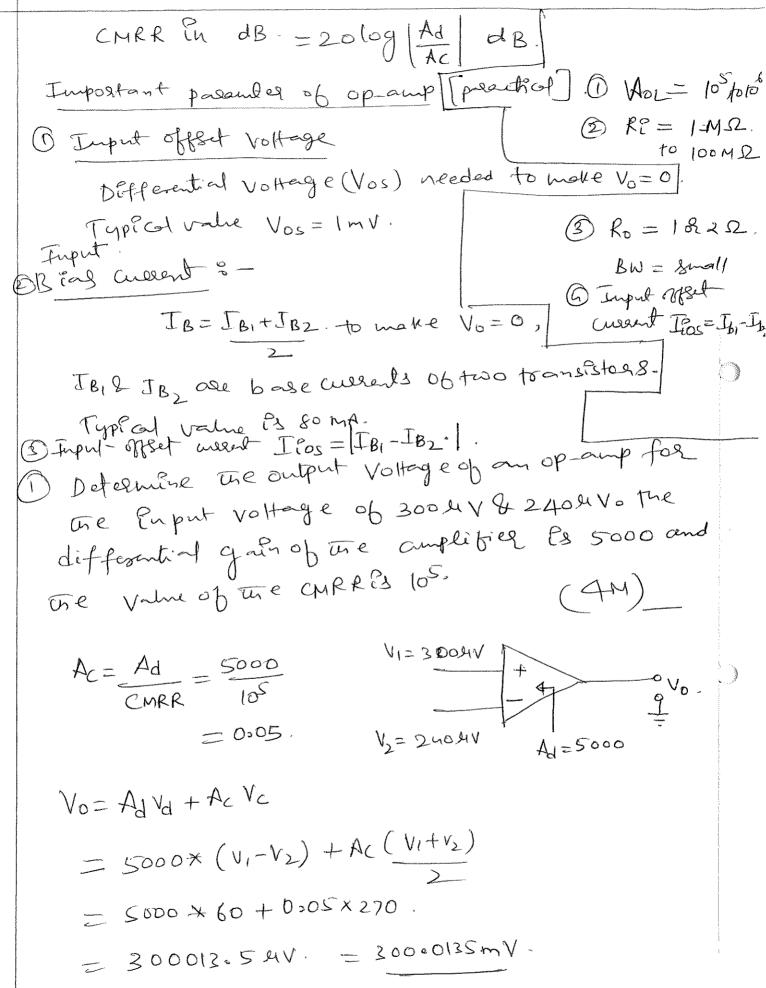
Vod (Vg-VA) Differential gain (Ad) From eg m O, we Com write  $V_0 = Ad(V_2 - V_2)$ Ad > Constant of propostionality The Ad P3 the gain with which difference between two Enput Signols. DoA o amplifies the hance it a different of gain. Ad. let differen Voltage Va= 1g-Vz. Hence differential gain = Ad = Vo Differential gain En decibel (dB) TAd= 2010910 (Ad) EndB-Common mode gain. (Ac) . If we apply two Emput Voltages which are equal En all the respects to the differential amplified Ele V1= V2 then Edeally the output voltage must be

egnal to zero.

CMRR = S= Ad Ac

Ideally  $A_c = 0$ , hence CMRR = 00.

Nrs. Ashark Asst. Professor, Ad is large, Acis Small, hence CMRR = large 2018-19



we know that

if we know Ad, Vc, Vd & CMRR we cam easily calculable Vog with out knowing Ac > Common mode voltenge gents.

Slow Rate and Foregramy response

Flegreny response.

Some RC Complings are provided an anop-amp cientit so as to reduce the gain at high frequencies.

otherwise, of positive feedback occurs from strang Capacitances consing high frequency Oscillations.

The op-amp acts like a Low-part filter with a

break frequent at fr=10Hz=

Typical fragueny response Es snown in fig using Bode pot.

From Bode plot

dB(A)= (00 + 3 dB.

Op-amp LPF Afr=for = unity gain(odb)

Mrs. Asha K, Asst. Professor fraymeny = Const SXIT.

frequery response. 2018-19

Afr = gain Boundwildts product

If regalive feedback around op-amp it geomis The gain to AF, then

$$\oint_{H} = \underbrace{f_{T}}_{AF} >> f_{n}.$$

Due to Reduction Engain Could by Feedback, the bandwedter Encocases from fin toft.

Slew Late: -

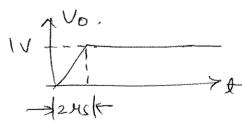
Because of presence of Capacitances, which is RC Combi tor Et com marge at a limited late, & the hate of mange 06 output of the op-amp & Cemited to

Its typical value is out V/ lis as shown in figure

For a Simusordal Biguel

Vo= Vm SEn W.

& I+B a combination of frequeny & peak value of output.



effect of slew late

The Two assumptions are.

10 Zero Enput allert 3-The current dead by esterer of the Exput terminals (Enverting & non Enverting) Es Zeao.

2. VERTUR Ground.

The means that differential comput vig Vd blow hon investing & exertially zero. Envesting Enput telements is exertially zero.

Ef Vo=few. volt8, due to læge open loop gain of op-amp,

 $V_d = 0 \cdot = V_1 - V_2$ 

Vo=Vd AOL E, e Vd = Vo = O, AOL= Veryling

 $V_d = (V_1 - V_2) = 0$ 

Trus andel lineal rouge of operation there Bursthaley snort aquit between are two Emput Learninals, un are sense that their voltages are same.

Fig shows the concept-06 one vistney grounds the queck line Endicates one Vistual shoot clement between ore Enput ternévals.

VIO Vistuals Conceptor virtual

· NOW Et the non-Enverting terminal & grounded by the Concept of vistnel ashort, the Enverting terminal is also at ground potential, trough tree Es Ono puystears Connection blu the Enterting terminal & the ground. quis le priniple of virtuel ground.

Mrs. Asha K. Asst. Professor between the MOSVIT put terminal & Zego. 2018-19

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#### Investing op-amp aquits. An amplifier which provides a phase shift of 180° between Expert & output is called Enverting amplifier. . The basic assuit déagram of an Enverting amplifier Es shown in figure. Connect Exput Signed Vin to the · non-Enverting teaminal Through a resistor R1. The non Enverting terminal is grounded. · The resistance Re Connects the output teeminal to investing terminal to provide the negative feedback. Note: - all amplifier should have negative feedback. when (+) telminal is grounded, the (-) telminal is Vistually at ground potential. steple vig at vy terminal. V=0 because consulted grown be cause consuted ground The Enput impedame of op-amp is Rin = as hence current into an op-amp teeminal & zero. From Vartual grount Concept V,=0. Here $I_f = \frac{V_1 - V_0}{R_f} = \frac{-V_0}{R_f}$ KCL to Enveeting Step 4 is went by ohns law $I_1 = \frac{Ve_n - V_1}{R_1} = \frac{Ve_n}{R_1}$ teaming 0-Vo = Vin The gain is. AV = Voltage Vo = - RF grag. Vin Ri Here are output voltage & the Vo = - (Rp) Vin regative of the Enput voltage, the it is Enveeted. ->Time t Waveform of Enverting Dhale shift

°6 180° SVIT

time t

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amplifier.

Phoblem (1)

An Enveling amplifier has  $R_1 = 2 \, \text{K} \, \text{R}_2 = 10 \, \text{K} \, \text{R}_3$  for an Enput Voltage of 105 V, find the output Voltage of the ciquit.

R, = 2KI Rf = 10KI VEn = 1-5V Vo = ?

$$V_0 = -\left(\frac{R_f}{R_1}\right) \cdot V_{ly}^2$$
$$= -\left(\frac{10 \times 10^3}{2 \times 10^3}\right) \times 105.$$

Design on investing amplifier to provide an output voltage of -9 v for an input of av.

given  $V_{i,j} = 2V$   $V_{0} = -9V$ Find RI, Rz.

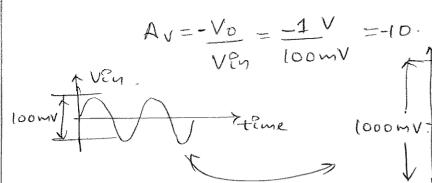
$$Av = \frac{Vo.}{Vin} = \frac{-9}{2} = 4.5.$$

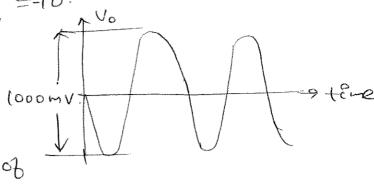
 $AV = -\frac{RF}{RI} = .$  Let RI = IKD

3. An op-amp & used as an anverting amplifier to amplifier on Enprt stree were of amplitude 100 mv. amplifier on Enprt stree were of amplitude 100 mv. (peak to peak) the input resistance R=1 ks and feedback resistance R=1 ks and feedback resistance Rf=10 ks. (almost the voltage gain & sesistance Rf=10 ks. (almost the voltage gain & sesistance Rf=10 ks.)

given: - Vin = coomV, R,=1KR Rg=1DKR. Av=?

$$V_0 = -\frac{R_F}{R_I} + V_{EN}^2 = -\frac{10 \times 10^2}{1 \times 10^2} \times 100 \text{ mV} = -\frac{1}{2018-19}$$
Mrs. Asha K, Asst. Professor





phase shift of

D'In are following op-amp agneët find voltage gain, Enput aussent (ausrent dawn) from the Source), output voltage, the west through the Load resistor. power delivered to the Load Desistor. 

given Data: -

Rg = 8K.

RI = 2K

R1 = 10052

Vin=105 V

Find Av, I'm Vo, IL, Po

$$Av = \frac{-Vo.}{Vin} = \frac{Rf}{Ri} = \frac{-8}{2} = -4.$$

$$P_0 = (V_0)^2 / R_L = (-6)^2 / 100$$
  
= 0.36 W.

$$I_L = \frac{V_0}{R_1} = \frac{-6}{100} = -0.06 A$$

Operational Amplifiera	(9)
Operational Amplifiers Non-Envertine amplifier	
Non-Lord	pleties The Enport without produced in Euport & output is called
An amplifier which implifier of amplifier of	e ant exactput Es called
1-0 any phase sono	n infra do
Non-Envertine amplifier.	
Nous Elion	Du En Kigure.
The circuit Diaglam is show	<i>(</i>
Input signal 3. applied to one how— Enverting boliminal. The registance Rf Connects one autout teaminal to Enverting	Ver=V1 +
Imput signal is applied to one	Vo.
hon-Envesting telming.	W XI
The registance Re Converts the	I RP IF
output teaminal to investig	Jankine :
The registance Re Connects the output terminal to provide the ne	egan
feedback.	01 70 R1
Feedback ciquet Es Completes	a sy central & @
and following of	
Step D Hage v. at the	non-Envesting teaminal.
The voltage vi on one	
Step Q. Ven = V,	
From the congt of Vietnas	ground, V1=V2=VEn.
step3)	Envering feeminal. Let I, is the
By applying the R	I The through the
Current a song resistor	Envering felminal. Let I, is the
South Class Dis	
Step @ Replace Cussent by ohn	nd ·
Step @ Replace cussed by ohn $\frac{0-v_2}{R_1} = \frac{V_2-v_0}{R_f}.$	$\Rightarrow \frac{-\sqrt{2}}{2} = \frac{\sqrt{2}}{2} - \frac{\sqrt{2}}{2}$
*I Rf.	KI KF Y.
	$\frac{V_0}{V_0} = V_2 \cdot + V_2$
	$\frac{V_0}{R_f} = \frac{V_2}{R_f} + \frac{V_2}{R_1}$
	CREEP 7 WILL
	$\frac{V_0 = V_2 \left[ \frac{R_I + R_f}{R_f * R_I} \right]  V_2 = V_1}{R_f * R_I}$
	$\frac{V_0}{R_f} = V_1 \left( \frac{R_1 + R_f}{R_f R_1} \right)$
	Rg [Rg Ri]
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Operational Amplifiers

Average 
$$V_0 = R_f \left( \frac{R_1 + R_f}{R_1 R_f} \right) = \left( 1 + \frac{R_f}{R_1} \right)$$

Ef R\_= to them [A\_V = 1] The act is them Voltage follower.

kravefolm of non-Envecting ventage complibies.

Ven Juput

No phase suite.

phoblems: -

Of non-Enverting amplifier has  $R_1 = 2KZ$ ,  $R_2 = 10KZ$ . for on input voltage of 1=5V, Find the output voltage of the white.

$$\frac{V_0}{V_{ey}^2} = 1 + \frac{R_F}{R_1} \qquad V_0 = \left[1 + \frac{R_F}{R_1}\right] V_{ey}.$$

$$= \left[1 + \frac{10}{2}\right] 1.05 = 9 V$$

$$A_V = \frac{Vo.}{V_{sy}} = \frac{9V}{1.5V} = 6$$

Design a non-Enverting amplified to paovede on output vottenge of av for an Enput of av.

given. Vo = 9V ·Vin = 2V.

$$A_V = \frac{V_0}{V_{in}} = 1 + \frac{R_F}{R_I}$$

$$\frac{9}{2} = 1 + \frac{Rf}{RI}$$

4 R1=1K1.

Re = 3,5 KSL

RISIKS.

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The open Loop Voltage gain of op-amp Es Av and due to finite gain the concept of vixtual ground Cannot be used.

& Vo = Av Vd = Av (ven-Va) -> 1.

Here Ry & R, forms a voltage dévêder.

$$V_g = R_1 + \frac{V_0}{R_1 + R_f} = \beta V_0$$

$$\beta = \frac{R_1}{R_1 + R_f}$$
 = feed back factor.

Vo = AV [VEn-BVO]

Vo = Av Ven - Arb Vo. Ce Vo(1+ Arb) = Arven.

But Vo & Called World Loop Voltage gain denoted asking

Voltage follower: -

A ciquit En which the output voltage follows the Enput voltage is called voltage follower ciguet. A voltage follower is a aimit with non-Envesting Configuration. The voltage gain es unity.

· Input signal Vi Ps Connuted to the now Envering termind

Voltage follower. · The output terminal

Mrs. Asha K. Asst. Professor Envering terminal disatistifo provide the negative feedback. The the following op-amp ciement find voltage gain, cussent dawn from the source, output voltage, the welent through the Load resistor. power delivered to the Load resistor.

given. RIZAKIL Kt = 8KV Vin = 25 En wt =258mpt.Eno III SRI SIP

Find Av, I'm, Voit Po

 $A_V = 1 + \frac{R_f}{R_I} = 1 + \frac{8}{2} = 5$ .

Ien = Vin = 2: = 1 mA (peak value).

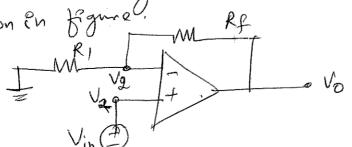
Vo = Av Vin = (5) 2 = 10 V

Vo(8ms) = Vo = 10 = 7.07 V.

po =  $\frac{Vo^2}{RL}$  =  $(7.07)^2/100 = 0.5$  Watts.

Draw the non-Enverting Voltage amplifier against using on op-amp & snow that the closed loop voltage gren is given by Aut = AV 1+AVB When Av > open loop

As: The non-Enverting amplifier is sum en figure.



vo Heye going B-> feedback

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StepOthe voltage V, at non-Envesting terminal (3 Vi=Vin

steppe node VI is also at the sque potential as va E, e Vin according to the consept of viertual ground.

 $V_1 = V_2 = V C_{in}$ .

Step The one node v2 & connated to the output terminal disety, the voltage at the output terminal is some as the Proofing terminal.

? Vo = V, = VQ.

It is also colled source follower, unity gain amplifier, buffer amplifier or Esolation amplifier. The output voltage is said to be following the Papert Voltage : o the august is colled a voltage follower.

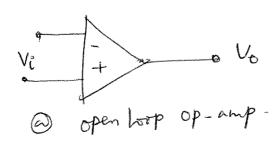
The waveform snown in figure.

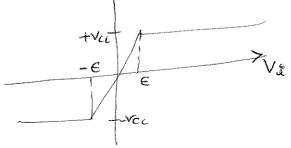
· Voltage follower has large bandwidth.

· Very large input resistance, in Ms. Vo . Low output impedance, almost 2000. Vm of . The olp follows the input exactly of without any phone shift.

Thomsfer characteristics of op-amp.

An op-amp & lineag with high gain over a very Small Value of Vi= € as shown in fig. beyond which it Saturates, Vo = Vcc





(b) Transfer characteristics

prollend the input to the op-amp is 1052 10t volls Draw the output waveform Enditching time pealed & maximum Value 1/2/18

Ans: - the cut is following

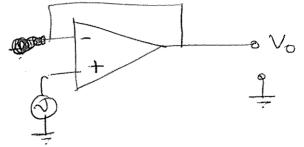
Vo = V24

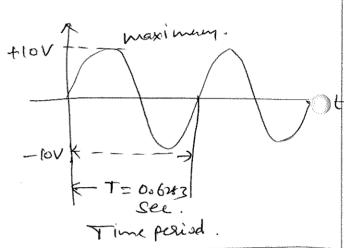
= 105 En 10 t.

maximum Value = 10V

 $\omega = 10 = 2T$ 

T = 0.6283 Seec.





Addition or Summer aquit :-

An op-amp went En which the output voltage & paoportional to the sum of the all the Enput voltages com be défined as summer ciquet.

Two types of sommer cigarit

1 Investing Summe aquiet

D Non Envering Summe cieuret.

Classification made dépending upon tre signof tre output.

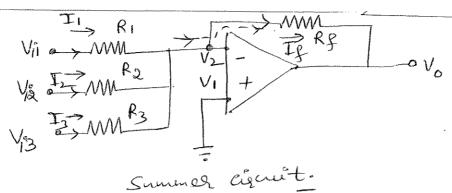
Investing Summing amplifier

· In this against, all the Expirt signed to beadded are applied to the Enverting Enput teaminal of the op-ourp- The circuit with three input signal

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Step 1: The nonintating teaminal is grounded is V,=0. Step 2: - using the concept of vatual ground, the voltage V2 at the Enverting teaminal B equal to V,

$$V_a = V_1 = 0$$

From KCL " At the investing terminal

KCL states orat ore Sum of the cullent's entering a terminal

 $I_1 + I_2 + I_3 = I_f.$ 

Step 4: - Replace each cultent by oum's law. must be earl to the terminal!

$$\frac{V_{21}^2 - V_2}{R_1} + \frac{V_{12}^2 - V_2}{R_2} + \frac{V_{23}^2 - V_3}{R_3} = \frac{V_2 - V_0}{R_5}; \text{ put } V_2 = 0.$$

$$\frac{V21}{R_1} + \frac{V12}{R_2} + \frac{V23}{R_3} = \frac{-V0}{R_5}$$

let R1=R2=R3=R.

if R=Rf.

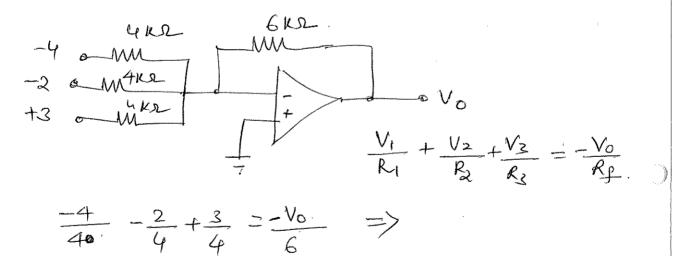
The significance of the negative sign is that the Eupont signed & output Signels are out of phase by 150°. psroblem: O'Calculate the output of Summing amplified when  $R_1 = 200 \text{K}\Omega$ ,  $R_2 = 250 \text{K}\Omega$ ,  $R_3 = 500 \text{K}\Omega$   $R_f = |000 \text{K}\Omega$   $|000 \text{K}\Omega|$   $|000 \text$ 

$$\frac{V_{21}^{2} + V_{32}^{2} + V_{33}^{2} = -V_{0}}{R_{1}}$$

$$\frac{-2}{200} + \frac{2}{250} + \frac{201}{500} = \frac{-V_{0}}{1000}$$

$$\left[-0.01 + 0.008 + 0.002\right] \times 1000 = -V_0$$

2). Find the output voltage of the 3-Enput added against shown below.



$$6 \left( -1 - 0.5 + 0.75 \right) = -40.$$

$$6 \left( -0.75 \right) = -40.$$

3) Design a adder cifcuit to get on output voltage

Of  $V_0 = -(3V_1 + 4V_2 + 5V_3)$  when Se for 30 k.

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$$V_0 = -R_f \left[ \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

$$V_0 = -\left[ \begin{array}{ccc} \dot{V_1} & \frac{R_1}{R_1} + V_2 & \frac{R_2}{R_2} + V_3 & \frac{R_2}{R_3} \end{array} \right] \rightarrow \boxed{2}$$

By composing egn 0 & 0

$$\frac{R_f}{R_1} = 3 \quad \frac{R_f}{R_2} = 4 \quad \frac{R_f}{R_3} = 5 \quad \text{let } R_f = 30 \text{ K}.$$

$$\frac{30}{R_1} = 3$$
  $\frac{30}{R_2} = 4$   $\frac{30}{R_2} = 5$ 

$$R_1 = 10 \text{K}\Omega$$
  $R_2 = 7.5 \text{K}\Omega$   $R_3 = 6 \text{K}\Omega$ 

inverting sunnel wear Rg = 1 ks

RI=IKR , B=2KR , B=3KR 4=4V V2=-2V V3=4V

$$V_{0} = -\left[\frac{R_{f}}{R_{1}}V_{1} + \frac{R_{f}}{R_{3}}V_{2} + \frac{R_{f}}{R_{3}}V_{3}\right]$$

$$= -\left[\frac{1\times10^{3}}{1\times10^{3}} \times 4V + \frac{1}{2} \times(-2) + \frac{1}{3} \times 4\right]$$

$$= (4V-1V+0.333V) = 4.33V.$$

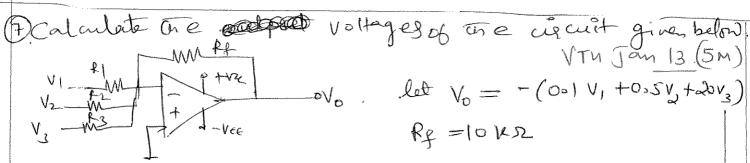
Détamine tre output voltage of the opéamp VIU: June 12. 4Mars. agaiet shown below.

$$-6 \times 0 = -\frac{1 \times 2}{1 \times 2}$$

$$+5 \times 0 = -\frac{1 \times 2}{1 \times 2} = -\frac{1}{2} \times (-6) + \frac{2}{3} \times (-6)$$

$$= -\left(\frac{2}{1} \times (-6) + \frac{2}{12018 - 19} \times 8\right)$$

**SVIT** 



The output of Enverting symmet is  $V_0 = -\left[\frac{R_1}{R_1}V_1 + \frac{R_2}{R_3}V_2 + \frac{R_2}{R_3}V_3\right]$ 

= -00/V,+005/2+20/3.

Rf = 001 Rf = 005 Rf = 20. y Rf = 10KR.

Rf = 10KR, R, = 100KL B=20KL, R3 = 0.5KR.

Non-Enverting summing aquiet.

Non-Enverting summing aquiet.

Here multiple input signals are commented to the non-Enverting terminal - Each Enput signal is connected to a seperate resistor.

The output teamined is connected to investing teaminof through a resistor. Rf: it provides negative feedback. The investing teaminal is also Connected to ground

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Q\/IT

Step1: The voltage V, at the non-investing Leani na).

many Enpuls are Connected to the non-investing tourish The voltage V, found by applying KCL. KCL states and some allert leaving the terminal.

 $I_1 + I_2 + I_3 = 0.$ 

let RI=R2=83=R.

$$\frac{V21-V1}{R} + \frac{V22-V1}{R} + \frac{V23-V1}{R} = 0$$

$$3V_1 = V_{31} + V_{02}^2 + V_{13}^2.$$

Vo Hage I step 2: using the Concept of usatual ground, the V2 at the Enverting learning is upred to V1.

Step 3: - apply KCL at the Enverting toeminal. Let It ) If are the account throngs bresistous R, Rf

Step4: - Replace each cuesant by ohm's (aw).

 $\frac{O-V_2}{R} = \frac{V_2-V_0}{\text{SVIT } R_{\text{g}}}$ 

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$$\frac{-V_2}{R} = \frac{V_2}{R_f} - \frac{V_0}{R_f}$$

$$\frac{V_0}{R_f} = \frac{V_2}{R_f} + \frac{V_2}{R}$$

$$\frac{V_0}{R_f} = V_2 \left[ \frac{R + R_f}{R_f + R_f} \right]$$

$$V_0 = V_2 \left[ \frac{R + R_f}{R_f + R_f} \right]$$

$$V_0 = V_2 \left[ \frac{R + R_f}{R_f} \right]$$

$$V_0 = V_2 \left[ \frac{1 + R_f}{R_f} \right]$$

$$V_0 = \left( \begin{array}{c} V_{21} + V_{22} + V_{23} \\ \end{array} \right) \cdot \left( \begin{array}{c} 1 + \frac{R_f}{R} \\ \end{array} \right).$$
If  $R_f = 2R_1$ , Then  $V_0 = V_{21} + V_{22} + V_{23}$ 

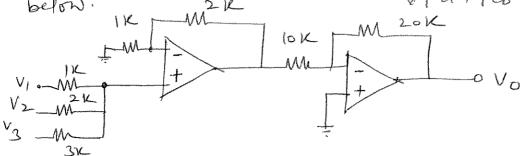
 $V_0 = \left\{ \frac{V_{c1} + V_{i2} + V_{i3}}{3} \right\} \left( 1 + \frac{R_f}{R} \right)$ 

$$V_0 = \frac{0.9}{3} \times \left[1 + \frac{10}{2}\right]$$





Calculate the output voltage of the ciguit given in VTu, Feb-09, (8M) big. below.



$$V_1 = 1V , V_2 = 2V , V_3 = 3V$$

Sot": By using super position Georem, & eonsider each Enput acting seperately.

case (D. V, acting V2 & V3 grounded.

This is non vinverting amplified with RETER , REIKE

 $\frac{1}{2} \lim_{n \to \infty} 2 \ln n = \frac{2 \times 3}{2 + 3} = \frac{6}{5} = \frac{102 \ln n}{2}$ 

$$V_B = \frac{V_1(2k\Omega 113k\Omega)}{1*k\Omega + [2k\Omega + 3k\Omega)} = \frac{V_1 * k2 k}{1*k + 102 k}$$

$$V_{01} = \left[1 + \frac{R_F}{R_1}\right] V_B$$
.  $V_B = 0.5454 V_1$ 

$$= \left(1 + \frac{2}{1}\right) * 0.5454 V_1 = 1.6363 V_1$$

Case @: - v2 quing VILV3 grounded. IKR 113KR=750R.

$$V_{02} = \left[1 + \frac{R_f}{R_1}\right] V_B = \left[1 + \frac{2 \times 10^2}{1 \times 10^3}\right] 0.2727 V_2$$

= 0.8181 V2.

Case 3: - V3 acting V, 2 v2 grounded, 1K2 11 2K2 11 = 666-6752

$$\frac{1}{6} \cdot V_{03} = \left[1 + \frac{R_P}{R_1}\right] V_B = \left[1 + \frac{2 \times 10^3}{1 \times 10^3}\right] \times 0.1818 V_3$$

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1 Vo3 = 0.5454 V3

Now the voltage ( $V_{01} + V_{02} + V_{02}$ ) is applied to Enverting ferminal of amplifies

( $V_{01} + V_{02} + V_{02}$ )

( $V_{01} + V_{02} + V_{02}$ )

( $V_{01} + V_{02} + V_{03}$ )

$$V_1 = |V_1 V_2 = 2V V_3 = 3V.$$

$$V_0 = -9.8|78 V$$

Subtractor or Difference amplifier vru, Ang 04,05 (M-S.)

The aquet déagram of Subtractor

one of the Enpit

Voltage is Connected to VII

the non Enverting teaminal

through a potential divider

metwork Roand R. as shown

in figure.

VEZ COMMENTAL OVO
VEZ COMMENTAL OVO
VEZ COMMENTAL OVO
VEZ COMMENTAL OVO
REZ MRZ
RZ
RZ
RZ
RZ

Difference amplifier.

- Another Enport voltage Es connected to the Enverting terminal through a resistor R1
- The resistor Re Connects the output teaminal to Enveeting questlesminal to provide negative feed back.

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SVIT

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Step1: - At the non-Enverting teaminal, two resistor are Connected, que voltage across one of the resistor is found by applying voltage divides onle.

$$V_1 = V21 \frac{R_3}{R_2 + R_3}$$

step 2: - using the concept of Victinal ground, the voltage Va at the investing teaminal B egrated to the voltage at mon investing teaminal.

$$V_{2} = V_{1} = V_{21} + \frac{F_{3}}{F_{2} + F_{3}}$$

Step3: By applying KCL at the Enveding teaminal. Let I, I are the aurent through restators R, Rg.

$$I_1 = I_f$$
.

Step4: Replace the each week by ohm's lan.

$$\frac{V_{u_2}-V_2}{R_1}=\frac{V_2-V_0}{R_5}$$

$$\frac{V_{u2}^2-V_2}{R_1}=\frac{V_2-V_0}{R_2}$$

$$\frac{V_0}{R_f} = \frac{V_2}{R_f} + \frac{V_2}{R_1} - \frac{V_0^2}{R_1}$$

$$\frac{V_0}{R_f} = V_2 \left[ \frac{R_f + R_1}{R_f \times R_1} \right] - \frac{V_0^2}{R_1}$$

$$V_0 = V_2 \left[ \frac{R_f + R_1}{R_1} \right] - V_Q \frac{R_f}{R_1}$$

$$V_0 = V_{1}\left(\frac{R_3}{R_2+R_3}\right)\left(\frac{R_1+R_1}{R_1}\right) - V_{12}^{2} \cdot \frac{R_2}{R_1} ; let R_3 = R_1 R_2 = R_1$$

$$V_0 = V_{11} \begin{pmatrix} R_1 \\ R_1 \end{pmatrix} \begin{pmatrix} R_2 + R_1 \\ R_1 \end{pmatrix} - V_{12} \begin{pmatrix} R_2 \\ R_1 \end{pmatrix} = \frac{R_2}{R_1} V_{11}^2 - V_{12}^2 R_1$$
Professor

Professor

If RE=RI, the voltage gain becomes unity, then the aquit les sobtraites circuit.

If Rf >R, then voltage gain becomes greated than runity and are aguet is Colled difference amplifier.

paublem.

Offor one given op-amp against find one output voltage.

Frake Rg=R3=12KR R1=R2=3KR, VE1=2.1V, VE2=0.7V.

que given ciqueit & a difference amplefier.

$$V_0 = \frac{R_F}{R_I} \left[ V_{C_I} - V_{C_2} \right]$$

$$=\frac{12K}{3K}\left(20+60.9\right)=12V.$$

Dosign a snitable aquit to realize une given expression Vo = 0.4V, -8 /2. There V, & V2 are the Enpot voltages Draw the ciqueit.

The expression for the output Voltage is

$$V_0 = \frac{R_3}{R_2 + f_3} \left( \frac{R_1 + R_f}{R_1} \right) V_1 - \frac{R_f}{R_1} V_2$$

|Rf = 8| |Rf = 8RI| let  $R_1 = 10KR$   $R_2 = 80KR$ . Comparing are coefficient of VI we get.

The coefficient of VI we got
$$\frac{R_3}{R_2 + R_3} \left( \begin{array}{c} R_1 + R_1 \\ \hline R_1 \end{array} \right) = 0.4 \cdot \frac{R_3}{R_2 + R_3} \left( \begin{array}{c} 10 + 80 \\ \hline 10 \end{array} \right) = 0.4$$

Mrs. Ashlers Asst. Professor = 0.0+4 >  $\frac{R_2+R_3}{R_1}$  SVIP2 2 0 72 [+  $\frac{R_2}{R_3}$  = 22.72 |  $\frac{R_3}{R_2}$  = 21.72[8-19]

3Design an p-amp aquit to get the required Expression Vo = 8 (V1-V2). -> 1

Since the 2 Enput voltages are subtracted , The Juguised ciquit is as follows.

Since the coefficient 06 V, & V, ale

gune.

Choose RI=R2

RR=R3.

$$V_0 = \frac{Rf}{R_1}(U_1 - V_2) \longrightarrow 0$$
By Comparing eqn  $\oplus$  80

 $\frac{Rf}{R} = 8 \quad Rf = 8 \times R_1 \quad \text{let} \quad R_1 = 10 \text{ kp}$   $\frac{Rf}{R} = 80 \text{ kp}$ 

Design treop-amp aquet which can give the output  $V_0 = 2V_1 - 3V_2 + 4V_3 - 5V_4$ 

The positive & negative teems Can be added seprestly using two adder then Subtraitog.

24, 7443, 7 Let Rg = 100KR.

$$V_{01} = -\left(\frac{R_{91} v_{1} + R_{11}}{R_{1}} v_{3}\right).$$

Comparing with P  $\frac{+RH}{R} = 2 \frac{R+1}{R} = 4$ 

R, = 50KIZ R3=2968.

3 V2 +5 V4, Let Rf2 = 120 KD

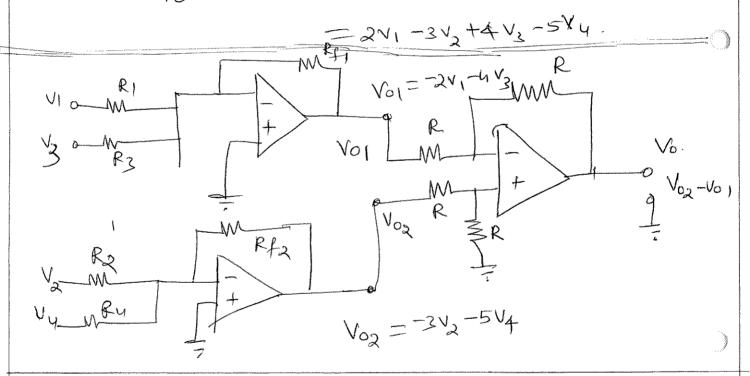
$$V_{02} = \frac{\left(\frac{R_{f}^{2}}{R_{2}}\right) + \left(\frac{R_{f}^{2}}{R_{4}}\right) V_{3}}{\left(\frac{R_{f}^{2}}{R_{4}}\right) + \left(\frac{R_{f}^{2}}{R_{4}}\right) V_{3}}$$

$$\frac{Rf_2}{R_2} = 3 \text{ have } R_2 = 40 \text{ K} \Omega$$

Rt2 = 5 hence R4 = 24 KR

use the subtractor with all the resistance of some Value of R=100 KR.

Here Vo = Voz -VoI, where Voz & VoI are the two Enputs of the subtractors



Litegrator: -

VT4 - mag 01,05 Feb 03,04

Time 13.

Any vigniet whose output voltage Es proportional to the Entegral of the Emph J-08-110 vottage can be déféned as an Entégeator.

A capacitor Es used for Rediging the Entegralor. The voltage across the Espacific Es.

Pc > B the week  $V_c = \frac{1}{c} \int \mathcal{L}_c \cdot dt$ Grough the Copnited 2018-19 Mrs. Asha K, Asst. Professor

Here are output voltage is Ri om Entegeation of the Enput, Vis MM voltage. . passère Enteglator Active integrator. The Enput Degnal & connected to the Enverting technical Through a resistance R. It is investing integental. · For the viguet to behave as on Entegrator, a Capacitor Es necessary. The apart for Es Connected En the
feedback pater. between the output teleminal & the . The non-Enverting terminal & connated to ground. Step 1:- The voltage VI at the non-Enverting technical Step 1:- The voltage VI at the non-Enverting technical & grounded VI=0. Step 23 - From the Concept of Viletud ground,  $I_1 = %$ stephi- seplace accent (by II) by Ohms (aw). Vi-0 - Ec RC = Vi

pre output voltage les Vo=-Vc. =- Islandt

 $V_0 = \frac{1}{\text{svij } R} \cdot dt = \frac{1}{\text{er}} \int V_3 \cdot dt$ Mrs. Asha K, Asst. Professor

Thus output Voltage & propostrond to one integral ob the input voltage & hence the ciquest Com be Colled Entegrator:

applications :-

In analog Computer Solvingare déférented equation In Your genelators

various signal Wave shaping aquits.

The semisoidal signal with peak value of 6 mv & 2 kbz.)

Flegueng is applied to the input of on ideal op-amp

Entegrator with R1=100KR, G=14F. Find the problem: -

output voltage For an Edeal Enteguish,

NOW RI = 100KR B. CF = IMF IVEN = Vm SENWIT

where Vin = 6 mV W=2 xf != 2xx x 103 x 2

$$= -0.06 \left( -\frac{\cos(u \times x \cdot 10^3 t)}{20 \times x \cdot 10^3} \right)^{\frac{1}{2}}$$

 $= 4.77 \times 10^{6} \left( \cos \left( 4000 \times 1 \right) - 1 \right) V$   $V_0 = 4.77 \times 10^{6} \left( \cos \left( 4000 \times 1 \right) \right) + 2018-19$ 

## Differentator: -

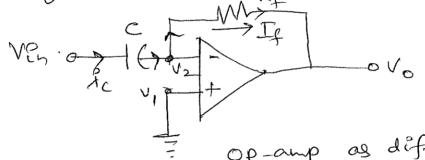
Any ciquiet whose output voltage is propostional to are desirative of the Expert voltage can be defined as a differentiator.

A capacitor Es used to realize the differentiator. The voltage acroll the Corporator Es

$$V_c = \frac{1}{C} \int dt dt$$

 $t_c = c \cdot d(v_c)$ .

Thus, are well through the Capacital is propostional to tre deliverive of the Capacitor yourge.



op-amp as differentator.

· Vin is connected to Enverting terminal through the Capacitor C. The Resistor Resi point between the output teeminal & the Enveeting textinal . The non-Enverting terminal Ps Connected to ground.

Step 7: The voltage Vi at the non-Enverting terminal Es V,=0, since non-investing tramend is grounded.

Step2: - Flomthe Concept of VEstual ground, the  $V_2 = V_1 = 0$ 

step3:- apply KIL at one investing termine). Let If is the current through resiston Rg & Let If is the Centrant through the Capaciton

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-appling differentialles

Replace the around by ohing law  $\frac{V_2-v_0}{Rf} = \frac{R_c}{R_c} = \frac{O-v_0}{R_c}.$ Pc = -Vo Re

The company of the contract of let vois the voltage across the aparitor

TVo=-RC.d(Vc)

Tro = -RC d (ven)

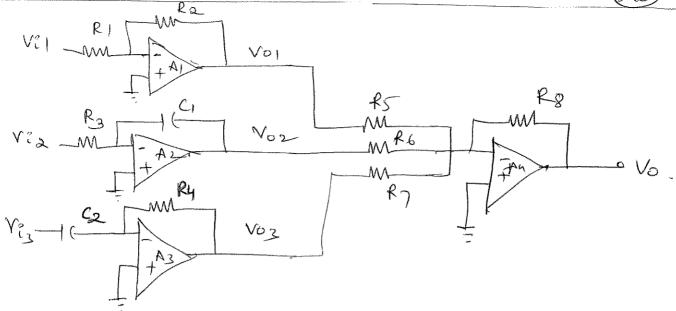
Thus, the output voltage & proportioned to the derivate of the Eupht voltage & have the Whuit cambe Called a different to 9.

-ve sign shows that the op-amp Es Committed as on Envering Configuration.

Problem Extra sloved Examples"

Forthe following aquet Find the expression for the output vollage.

given. R1=R2=R5=R6=R7=R8=1KS R3 = R4 = IMSL C1 = C2 = 1 Sef.



The op-amp A, is an Enverting amplified. Therefore one output of A, can be written as

 $V_{01} = -R_2 v_{01} = -V_{01}$ . The openh  $A_2$  is an Enverting integrator. The output of  $A_2$ 

$$V_{02} = -\frac{1}{R_3 C_1} \int V_{02}^2 dt$$

$$= -\frac{1}{1 \times 10^6 \times 1 \times 10^6} \int V_{02}^2 dt$$

$$= -\int V_{02}^2 dt$$

The opamp Az is an investing differentiation. The output

of Az is

$$V_{02} = -R_{11}C_{2}\frac{d}{d+}(V_{03})$$

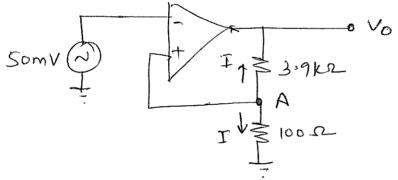
$$= 1\times10^{6}\times1\times10^{6}\frac{d}{d+}(V_{03}^{2})$$

$$V_0 = \frac{-R_8 \cdot \left[ V_{01} + V_{02} + V_{03} \right]}{R_5}$$

$$= \left[ -V_{11} + \left( -\int V_{12} \cdot dt \right) + \frac{d}{dt} \left( -V_{13} \right) \right]$$

$$= V_{11} + \left[ V_{12} \cdot dt + \frac{d}{dt} V_{13} \right]$$

D. Find the output & closed loop gain of the op-amp



Vin= 50mV.

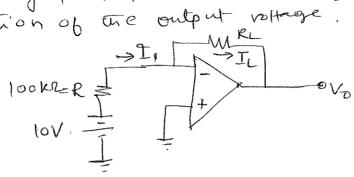
$$I = \frac{50}{100} = 0.5 \text{ m/A}.$$

No auent flows into are to teeminal

$$V_0 = V_A + 3.9 \times 0.5 \times 10^3 \times 10^3$$
  
=  $50M + 1950M = 2000MV$ .

AF = 
$$\frac{10}{10} = \frac{10}{10} = \frac{10}{10}$$

DINTE figure RL is the transducer resistance which can vary from 1 ks to 10 ks. Determine the lange of Variation of the output voltage.

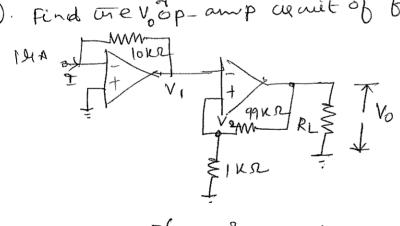


$$\frac{I_1 = I_L}{I_{00}} = -\frac{V_0}{R_L}$$

$$V_0 = \frac{-RL}{10}$$

RL=1KR, Vo=-0.1V } range.
RL=10KR, Vo=-1V.

3). Find tre voop-amp aquit of tigme below.



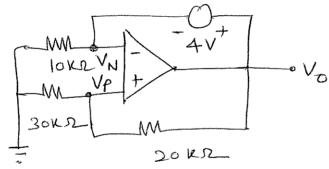
V1 = -1x10 x10x10 = -0.41V.

because vistual glound compt  $V_2 = V_1 = -0.0 |V_1|$ 

Applying KCL of node (2)

An op-amp has a slew laste of 0.8V/US. what Es the maximum amplitude of undistorted Sine wave that the op-amp Cam produce at a frequenty of 40KHz? What Op-amp is the maximum frequenty of the sine wave that op-amp is the maximum frequenty of the sine wave that op-amp can reproduce if the amplitude is 31?

For an op-amp us mit of figure below determine Vp. Vn. Vo and also power supplied absorbed by the 4V source.



$$V_p = 30. V_0 = 0.6 V_0$$

$$V_{N}+4=V_{0} \Rightarrow 0.6 V_{0}+4=V_{0}$$

$$V_{0}=10 V$$

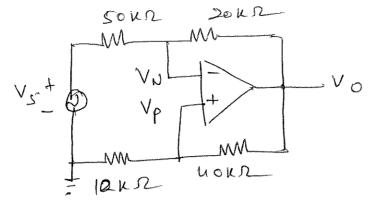
? (4 V source) = 0.6 m A entering at + reterminant

power absorbed = p = 4x006 mA

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For an op-amp we wit of Figure Find vo if  $v_s = 9V$ All registance are En KR.



Vp = 10. 0-2 Vo

VN= 0.2 Vo By applying KCL at VN node.

$$\frac{V_s - V_N}{so} = \frac{V_N - V_O}{20}$$

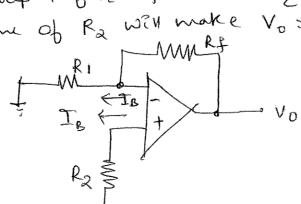
$$9 - 0.2 \text{ Vo} = 0.2 \text{ Vo} - \text{ Vo}$$

180 - 4 Vo = 100 - 50 Vo.

180 = 1000-50V0+4V0

180 = -360 Vo => Vo=5 K-

Fig belows shows the effect of bias well (Is,=Is=Is)
on the output box an Enverting op-amp cijuit.
what value of R2 will make Vo=0?



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$$V_{+} = R_{2} I_{B}$$
.

at  $G_{R} = V_{+} + V_{+} - V_{0}$ 
 $I_{B} = V_{+} + V_{+} - V_{0}$ 
 $R_{f}$ 

$$V_0 = 0$$
.
$$R_2 = R_1 \parallel R_F.$$

The two Emput voltages of own of amp all 2V& 3V= The Common output Voltage is 2 mV. the difference made olp voltage B 9V. Find CMRR.

$$V_1 = 2V$$
  $V_2 = 3V$   $A_C = A_D = ?$ 

$$A_c = \frac{V_{CM,O}}{V_{CM}?\eta} = \frac{2mV}{(2+3)/2} = 0.8 \times 10^{-3}$$

$$Ad = \frac{V_{dm.0}}{V_{dm.2n}} = \frac{9V}{(3V-2V)} = \frac{9}{2}$$

$$CMRR = Ad = 9/0.8x153 = 11250.$$

An operational amplifier has two april voltage. of 60 and 30. The difference made output voltage is Common mode voltage gain & total output voltage

Vid = 
$$V_1 - V_2 = 3V$$
 Ad =  $\frac{Vod}{Vid} = \frac{10}{3} = \frac{2.33}{3}$ .

Mrs. Ashark Asst. Prolessor =  $\frac{Ad}{AC}$ 
 $\frac{A}{2} = \frac{3.33}{100} = 1.21 \times 10^{-10}$ 



= 0.00149+9.99